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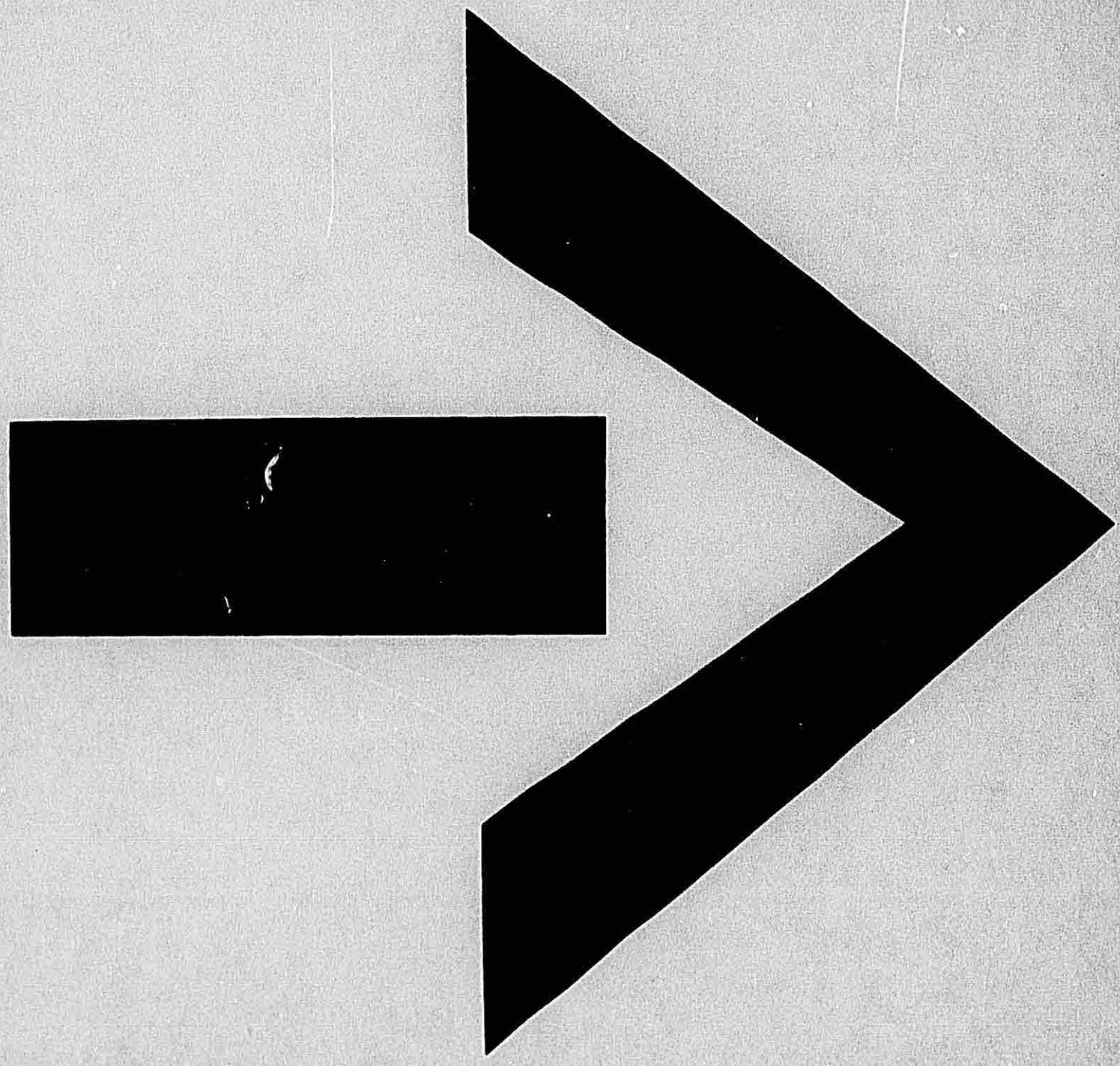
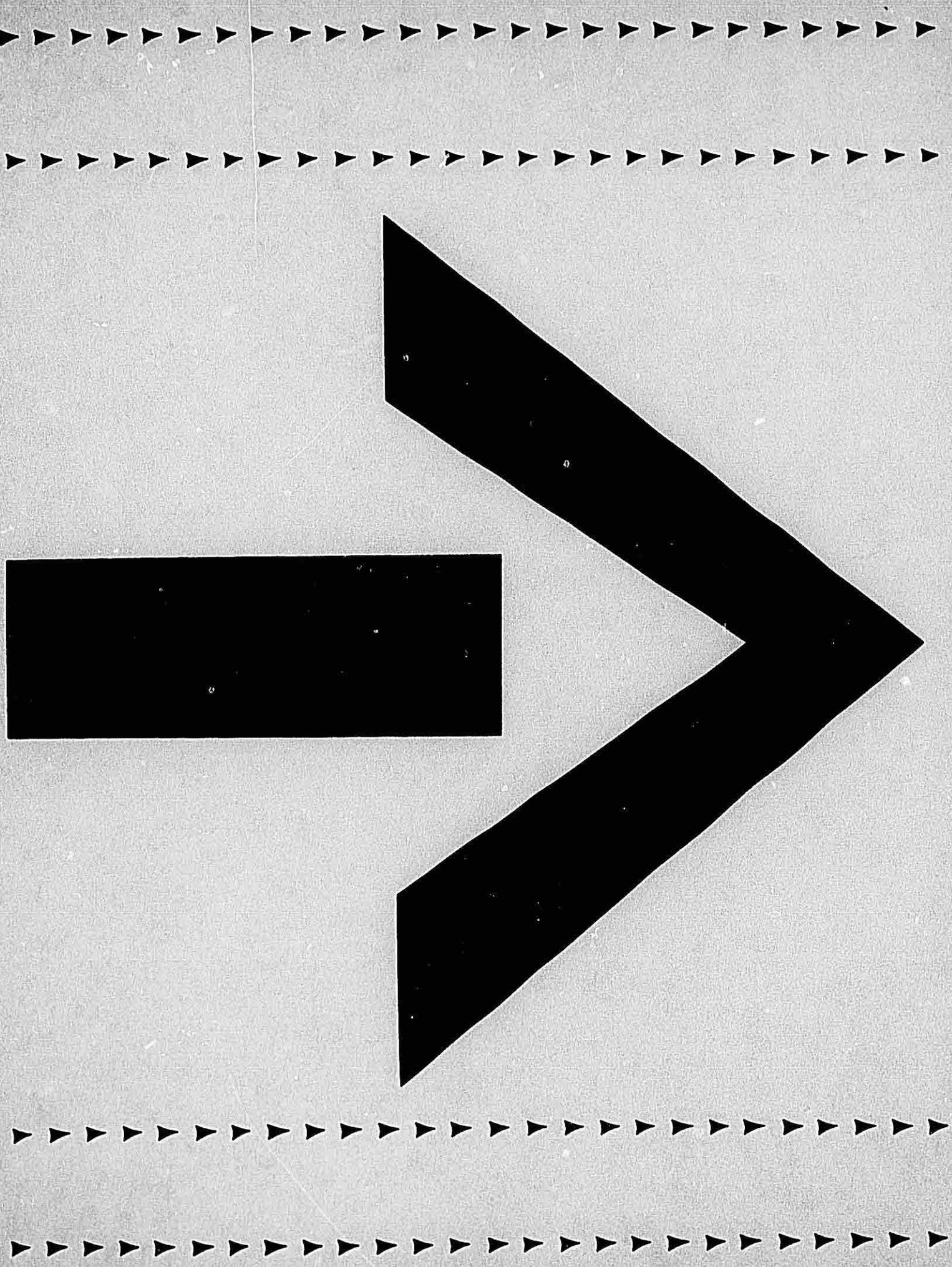




NARCO AVIONICS INC.

IDME 891 SYSTEM

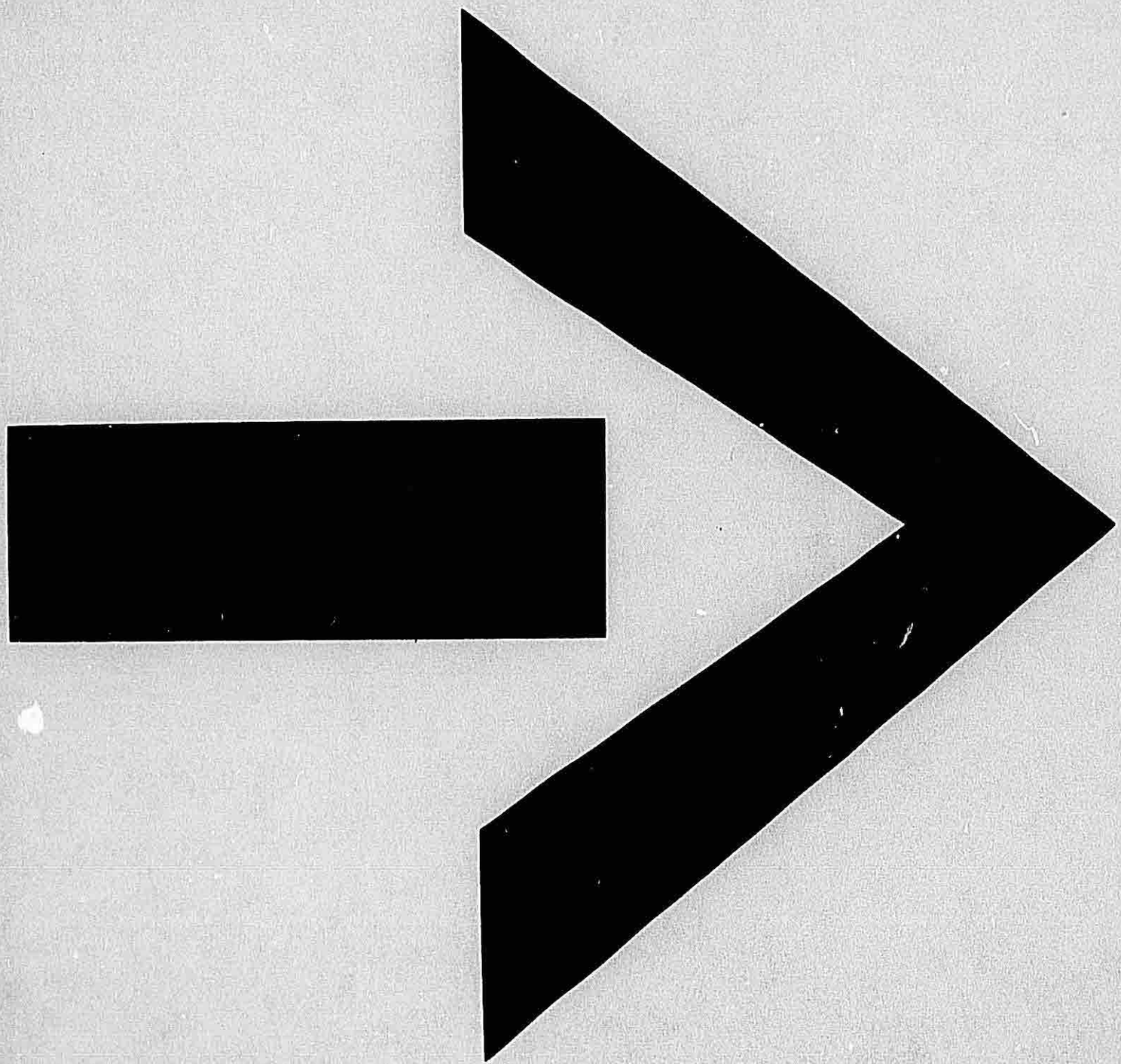
REMOTE CHANNELED DME WITH VOR-ILS INDICATOR

MAINTENANCE MANUAL

MANUAL PART NUMBER 03315-0600

NARCO AVIONICS INC
270 Commerce Drive
Fort Washington Pennsylvania,U.S.A,19034

Printed in U.S.A **April 1985**



RECORD OF REVISIONS

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NARCO AVIONICS IDME-891

MANUAL 03315-0600 dtd **April 1985**

IS YOUR MANUAL COMPLETE?

This page is provided, and updated as necessary, with each printing and supplement issued. As all pages are dated, it is easy to verify if the manual on hand is complete and current. Page numbers prefixed by a "B" are pages that are intentionally blank.

A complete page by page check can be made by comparing the page number and date below to that of each page. A quick check can be made by "eyeing" the bar(s) at the base of this page against the bottom edge of the whole manual. One bar on this page indicates one set of supplemental pages were issued, additional bars. . . additional supplements. Generally one will eye at least one bar per supplement.

It should be noted that the pages of Sections 1 and 2 may be dated prior to the cover date of the Maintenance Manual as those Sections are the Installation Manual which always preceeds the Maintenance Manual.

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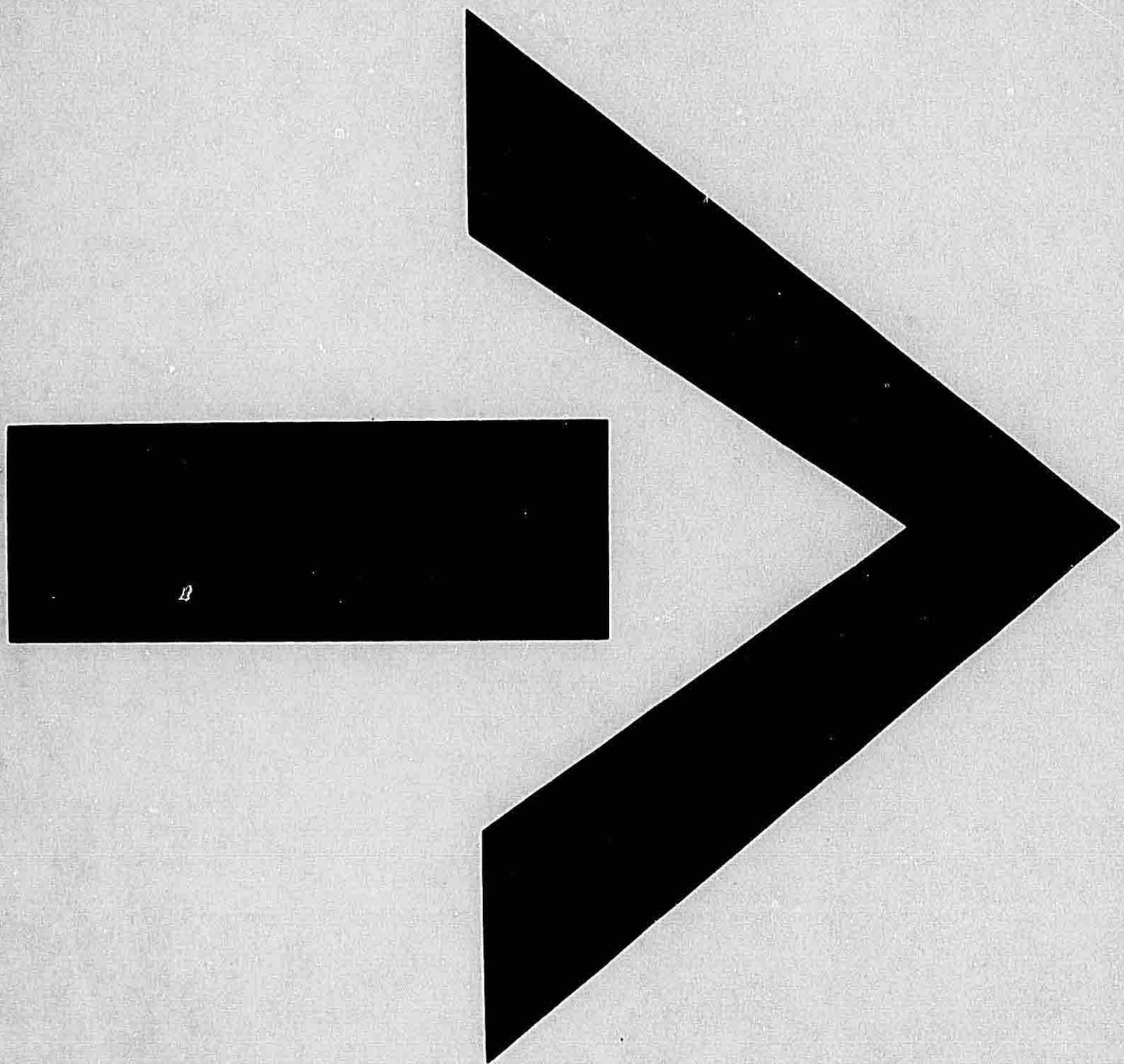


1.1. INTRODUCTION

In support of the Narco Avionics IDME-891 DME/VOR-ILS Indicator System, this manual provides detailed installation and maintenance procedures. This manual is intended for use only by persons who are qualified to service this equipment described in this manual persuant to current regulatory requirements.

1.1.1 MANUAL ORGANIZATION

Organized into six major sections, the manual provides the following:

SECTION 1 **GENERAL INFORMATION** --- Product description, ordering information, specifications, environmental category and licensing requirements.

SECTION 2 **INSTALLATION** --- Detailed information for performing the mechanical and electrical installation.

SECTION 3 **OPERATION** --- Operation of the IDME-891 system is covered only to the extent of making electrical tests necessary to confirm proper operation.

SECTION 4 **THEORY OF OPERATION** --- Technical description of electrical circuits.

SECTION 5 **MAINTENANCE** --- Provides test, alignment and troubleshooting procedures.

SECTION 6 **SCHEMATICS & ILLUSTRATED PARTS LISTS** --- Contains exploded views of mechanical parts, complete components parts lists, component layout drawings and circuit schematics.

NOTE: **INSTALLATION/OPERATION MANUALS CONTAIN SECTIONS 1, 2 & 3. MAINTENANCE MANUALS CONTAIN, IN ADDITION TO SECTIONS 1, 2 & 3, SECTIONS 4, 5 & 6**

1.2 PRODUCT DESCRIPTION

The IDME-891 is an independent remotely channeled DME receiver combined with a VOR-ILS indicator designed to be mounted in a standard 3-inch aircraft instrument panel opening. The unit is wedded normally to the NS-801 RNAV or the Narco MK-12D and NAV-824/825 series of NAV receivers as it relies on these receivers for DME channeling information and VOR-ILS converter outputs to drive the indicator's meters and flags. The IDME-891 operates from either 14 or 28 Vdc.

The Indicator portion of the unit displays the following:

1. VOR-ILS information in the form of standard meter and flag movements.
2. Marker Beacon information in the form of white, amber and blue lights that are driven by a remote mounted receiver, such as the Narco MKR-101 or CP-136M.
3. Digital DME distance and groundspeed information (not simultaneously) in the form of a high intensity Light Emitting Diode (L.E.D.) display. Groundspeed information is displayed when the VOR course selector knob is depressed.

VOR bearing selection is made by the indicator's course selector potentiometer.

1.3 DESIGN FEATURES

- 100% modular solid state design for ease of servicing.
- High intensity Light Emitting Diode (L.E.D.) DME digital display.
- Instant station lock-on, typically less than one second.
- Distance accuracy ±0.1 nautical mile (nominal) up to full range.
- Groundspeed accuracy ±5 knots or ±5%.
- 200 channels, 25 watts (nominal) transmitter.
- Manual DME display intensity control.
- Remote channeling only, no DME tuning controls.
- 11 to 32 Vdc power input operation, no voltage converter required.
- Compact, lightweight, self-contained.
- ARINC panel cutout, 3" instrument hole.
- VOR-ILS indicator provides a standard pivoted VOR/LOC meter movement and rectilinear glideslope meter movement.
- Marker beacon lights provided for remote mounted marker beacon receiver.
- Course selector potentiometer for VOR bearing selection.
- Wedded normally to the NS-801 RNAV or Narco MK-12D and NAV-824/825 series of NAV receivers.
- Compatible with RNAV-860 and NS-801 Area Navigation systems.

1.4 PRODUCT SPECIFICATIONS

A. MECHANICAL

SIZE:	IDME-891 Case	9 19/64" long x 3 3/16" wide x 3 3/16" high (229 mm) x (81 mm) x (81 mm)
SIZE:	IDME-891 Panel Cut-out	3 3/16" dia. (81 mm dia.)
SIZE:	UDA-3 DME Antenna	3 7/8" long x 7/8" wide x 3 9/16" high (98.5 mm) x (22.2 mm) x (90.5 mm)
WEIGHT:	IDME-891	2.6 lbs. (1.18 Kg.)
WEIGHT:	UDA-3 antenna/ 8 ft. cable	0.5 lbs. (0.21 Kg.)

B. ELECTRICAL

SUPPLY VOLTAGE: 11 to 32 Vdc
CURRENT, LESS PILOT LAMPS AT 14 Vdc: 0.6 ampere
CURRENT, LESS PILOT LAMPS AT 28 Vdc: 0.3 ampere
CURRENT, INDICATOR PILOT LAMPS AT 14 Vdc: 0.32 ampere
CURRENT INDICATOR PILOT LAMPS AT 28 Vdc: 0.32 ampere
CIRCUIT BREAKER RATING: 1.0 ampere

TRANSMITTER FREQUENCY BAND: 108.00 thru 117.95 MHz paired with 1041 thru 1150 MHz
TRANSMITTER POWER: 25 W nominal, 22W minimum
TRANSMITTER FREQUENCY STABILITY: less than .01%
NUMBER OF CHANNELS: 200
RECEIVER FREQUENCY: 108.00 thru 117.95 MHz paired with 978 thru 1213 MHz
RECEIVER SENSITIVITY: -82 dBm minimum
ACQUISITION TIME, INCLUDING CHANNELING: 1 second
RANGE: 0-160 nm
MEMORY TIME: 8-10 seconds
DIGITAL DISPLAY READOUTS: 160 nm in 0.1 nm increments
ACCURACY, RANGE: ±0.1 nm nominal, 0.4 nm maximum
GROUND SPEED ACCURACY: ±5 knots or ±5% (std. signal conditions)
IDENT AUDIO OUTPUTS: high impedance 47K (See Section 2.3.8)
low impedance 4.7K
VOR/LOC INDICATOR (Left-Right): 150-0-150mv/100 ohms
VOR TO/FROM FLAG: 90mv/100 ohms
GLIDESLOPE INDICATOR (UP/DOWN): 150-0-150mv/1000 ohms
GLIDESLOPE FLAG: 250mv/1000 ohms
MARKER BEACON BULBS: 5V/0.115 ampere

1.4 Continued

C. ENVIRONMENT	
Temperature Range	
Non-operating - low	-40°C (-40°F)
high	+70°C (+158°F)
Continuous operation	
high	+55°C (131°F)
low	-15°C (+5°F)
Altitude	
Non-pressurized	50,000 ft.
pressurized	50,000 ft.
Not affected by decompression to	50,000 ft.

1.5 ORDERING INFORMATION FOR UNITS AND ACCESSORIES

The following list identifies the IDME-891 system and the order number to use to obtain the complete system. Individual items of the system may be ordered using the part numbers listed opposite the individual item.

ITEM	ORDER NUMBER	DESCRIPTION	PART NUMBER
1	03315-0300	IDME-891 System, including Antenna & Installation Kit	
		INDIVIDUAL ITEMS	
		IDME-891 Unit only	01424-0101
		Antenna, UDA-3	01063-0102
		Installation Kit	03315-0500
		ACCESSORIES	
		straight connector hood	41307-0004

1.5 Continued

INSTALLATION KIT			
ITEM	PART NUMBER	DESCRIPTION	QTY.
1	41273-0002	Connector, BNC (Plug)	1
2	90072-0002	Cable, Coax, Low Loss, 8 ft.	1
3	41364-0008	Connector, 37 pin (P301)	1
4	41307-0008	Connector Hood, Right angle (P301)	1
5	41308-0008	Connector Locking Assy. (P301)	1
6	41372-0004	Connector socket contacts (P301)	37
7	81329-0108	Flat Washer for rear support stud	1
8	81324-0009	Lockwasher, split, for rear support stud	1
9	81193-0004	Wing nut, for rear support stud	1

1.5.1 ACCESORIES REQUIRED BUT NOT SUPPLIED

One of the following Narco Centerline II NAV receiver/converters are required to remote channel the IDME-891 and provide steering information to its VOR/LOC indicator:

a. MK-12D with VOR converter, NAV-824/825
b. NS-801 RNAV system
In addition, the following equipment may be added to complete the avionics system:
c. Glideslope Receivers: UGR-2A 2/5 with ARINC channeling, NS-801 RNAV, NAV-825 or MK-12D with glideslope to drive the GS needle and flag in the IDME-891 indicator.
d. Marker Beacon Receivers: MKR-101R remote-mounted marker beacon receiver or CP-136M audio panel with marker beacon receiver, to drive the marker beacon lights in the IDME-891 indicator.

1.5.2 MISCELLANEOUS ITEMS REQUIRED BUT NOT SUPPLIED

a. Sufficient length of #22 AWG stranded hook-up wire.
b. Three #6-32 x 7/16 lng. mounting screws for IDME-891 panel mounting.

1.6 LICENSING REQUIREMENTS

OPERATOR:

The Federal Communications Commission requires that the operator of the transmitter in this equipment hold a Restricted Radio Telephone Operator Permit, or higher class license. A permit may be obtained by any U.S. citizen from the nearest field office of the FCC; no examination is required.

1.6 Continued

AIRCRAFT:

The IDME-891, as installed in the aircraft, requires an Aircraft Radio Station License. This license is obtained by filing FCC Form 404. The unit may be operated for up to 30 days without a station license, after filing the FCC Form 404 and while awaiting receipt of the station license, providing a copy of the FCC Form 404 is kept in the aircraft. However, if the aircraft has been previously licensed for a DME, resubmittal of the FCC Form 404 is not required.

This equipment has been type accepted by the FCC and entered on their list of type accepted equipments as "NARCO IDME-891".

CAUTION

The UHF transmitter in this equipment is guaranteed to meet FCC approval only when a Narco crystal is used. The use of other than Narco crystals will void manufacturer's warranty.

2.1 INTRODUCTION

This section provides all the electrical and mechanical installation information. Electrical Installation and Mechanical Installation Sections are independent and self-supporting. This permits their removal from the manual allowing the electrical and mechanical installation efforts to proceed in parallel.

The IDME-891 Interconnect cable is to be constructed by the installing agency.

2.2 PRELIMINARY PROCEDURES

2.2.1 PRELIMINARY INSPECTION

Carefully unpack the equipment, noting any damage to shipping cartons or avionics. If damage is noted, retain the cartons to corroborate damage claims.

Inventory received items against the lists in Section 1.5 to assure complete order.

2.2.2 PRE-INSTALLATION BENCH TEST

The purpose of this sub-section is to determine that the unit meets factory performance specifications.

2.2.2.1 TEST EQUIPMENT REQUIRED

1. Power Supply, 10 to 30 Vdc at 1.5 amp.
2. DME Signal Generator, IFR 1200Y3 or equivalent.
3. Headphones, 500 to 1000 ohms.
4. VOR/ILS Generator, IFR Model N-750 or equivalent.

2.2.2.2 BENCH TEST SET-UP AND CABLE FABRICATION

The cable shown in Figure 2-1 will permit bench testing of the IDME-891 without its companion NAV receiver. Alternatively, the cable to be installed in the aircraft may be used providing, in addition, a checkout of avionics, cabling and calibration of the VOR-ILS indicator to the NAV converters.

Shown in Figure 2-1 is an arrangement whereby the popular IFR NAV 750 VOR-ILS generator is used to remote channel the IDME-891. The IFR NAV 750 offers 2-out-of-5 remote channeling from its rear panel accessory connector J8. Remote channeling is controlled by the front panel frequency select switches.

Other remote channeling sources for bench testing could be an independent 2/5 control head, DME generators with 2/5 remote channeling capability or NAV receivers with 2/5 remote channeling such as the MK-12D, NAV-824/825, NAV-124 or NAV-122.

2.2.2.2 (Continued)

Table 2.1 lists the IDME-891 channeling code. With the exception of the resistors shown in Figure 2-1, which must be supplied by the installing agency, a bench test cable may be fabricated by ordering from Narco the following parts:

QTY.	PART NUMBER	DESCRIPTION
1	41364-0008	37 pin connector (IDME-891 P301)
2	41307-0004	Connector hood for P301 and P8
2	41308-0004	Connector locking assy. for P301 and P8
1	41372-0004	Connector socket contacts (P301)
1	41368-0007	37 pin connector for IFR NAV750 (P8)

TABLE 2.1 IDME-891 2/5 CHANNEL PROGRAMMING

MHz ARINC	DME 891 P301	MHz CHANNELS									
		108	109	110	111	112	113	114	115	116	117
A	31	X	X		X	X					
B	12			X	X		X	X			
C	30					X	X		X	X	
D	11	X						X	X		X

KHz ARINC	DME 891 P301	KHz CHANNELS																			
		.00	.05	.10	.15	.20	.25	.30	.35	.40	.45	.50	.55	.60	.65	.70	.75	.80	.85	.90	.95
A	28			X	X	X	X											X	X	X	X
B	9	X	X	X	X			X	X	X	X										
C	27					X	X	X	X			X	X	X	X						
D	8									X	X	X	X			X	X	X	X		
Y Chan ACT	32		X		X		X		X		X		X		X		X		X		X

NOTES:

"X" indicates continuity to System Ground via NAV Unit.

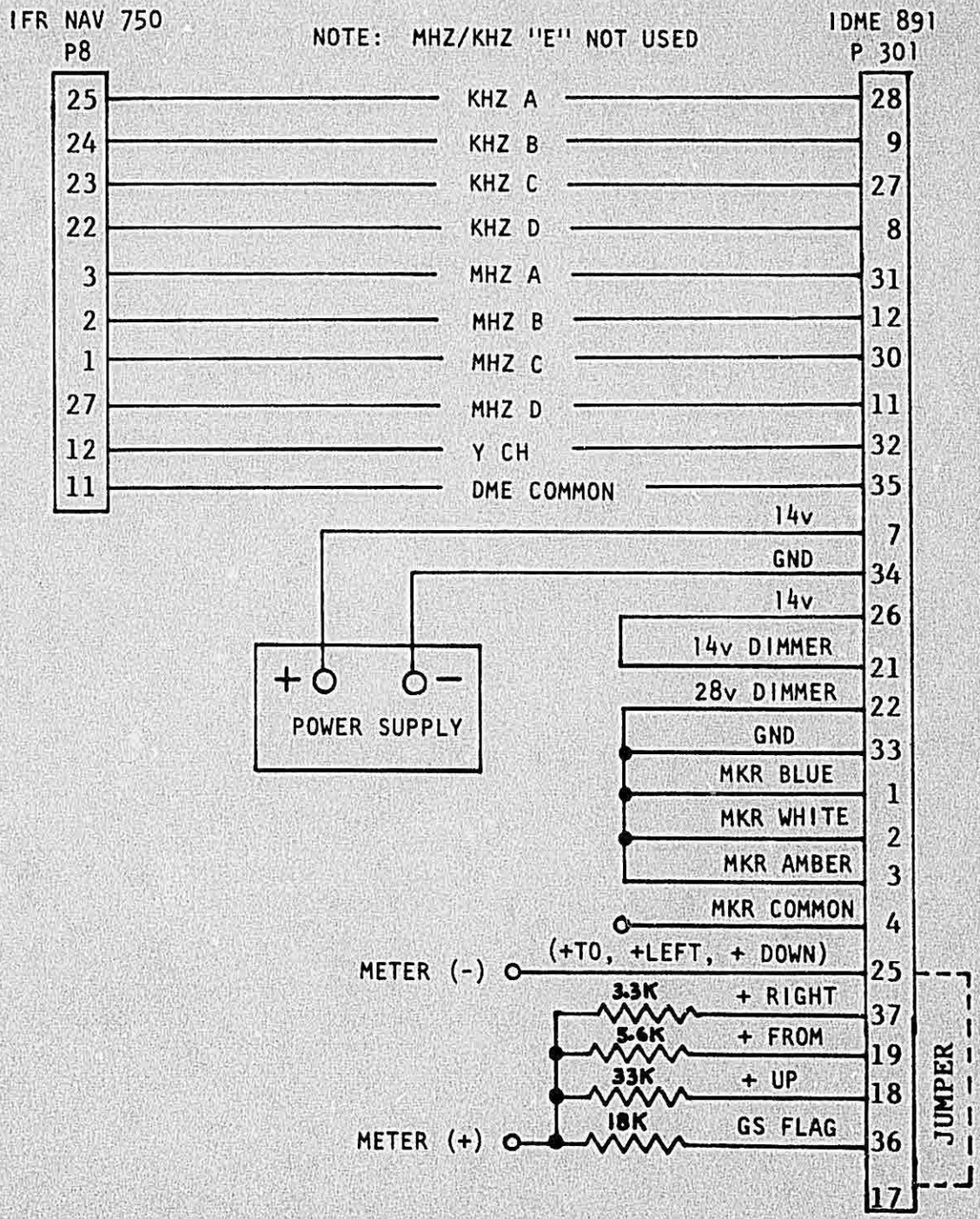


FIGURE 2-1 BENCH TEST HARNESS

2.2.2.3 BENCH TEST PROCEDURE

Before conducting the bench test, refer to Section 3 (OPERATION) to familiarize yourself with the IDME-891 operation.

The following bench test is conducted with a harness constructed as shown in Figure 2-1. However, if the aircraft's interconnect cable between the IDME-891 and its companion NAV converter(s) is used for the bench test, omit the VOR-ILS Indicator Test (Step B) and instead, calibrate the indicator as in Step D.

CAUTION

The VOR-ILS indicator section of the IDME-891 must be calibrated to its associated VOR/LOC and GS converters.

A. DME SECTION TEST

1. Turn IDME-891 power switch to OFF position.
2. Connect system for bench test as shown in Figure 2-1.
3. Set the DME test generator parameters as follows:

   RANGE: 100 nm.
   ATTENUATOR: -73 dBm
   REPLY EFFICIENCY: 70%
   SQUITTER: 2700
   FREQUENCY: 112.50 MHz
   IDENT: ON

4. Channel the IFR NAV 750 to 112.50 MHz
5. Set the power supply to 14 Vdc.
6. Turn the IDME-891 power switch to "ON" position.
7. Verify that the DME's distance readout is illuminated and reads 100 ±0.2 nm.
8. Set the DME test generator groundspeed to 240 knots, direction inbound.
9. Set DME test generator range switch to "velocity" position
10. Verify that the DME distance is smoothly tracking inbound in 0.1 nm steps.
11. Allow the groundspeed to stabilize a minimum of 5 minutes.
12. Check groundspeed by depressing the VOR course selector knob. The displayed groundspeed should be within ±5% of that indicated (240 kts) on the test generator.
13. Check sensitivity during tracking. IDME-891 should track at -82 dBm.
14. Remove the RF signal from the IDME-891. Verify that, in approximately 10 seconds, the DME readout displays BARS. Restore the RF signal.
15. Verify remote channeling of ALL KHz channels by checking for lock on as the IFR NAV 750 and DME test generator KHz frequency select switches are cycled from 0 to .95.
16. Verify remote channeling of ALL MHz channels as per Step 15.
17. Check the DME display dimming operation by rotating the dimmer control knob thru its full range.

2.2.2.3 **Continued**

18. Check transmitter power on all channels. Power should be 25W nominal.

CAUTION: Many DME test generators do not have the capability to accurately measure power as low as 25 watts.

NOTE: The digital system of the IDME-891 operates statistically on a TACAN or DME signal. Some test generators do not accurately simulate the ground DME or TACAN signal and may not operate the IDME-891 correctly. The result is improper distance or groundspeed computation. This is usually caused when squitter or countdown is not produced in a random manner.

B. VOR-ILS INDICATOR SECTION TEST

1. Turn the IDME-891 power switch to the OFF position.
2. Reset the power supply to 5.5 Vdc.
3. LEFT/RIGHT, TO/FROM, UP/DOWN, GS FLAG TEST

a) Touch the Meter (-) lead to the power supply negative terminal and the Meter (+) lead to the positive (5.5 Vdc) terminal. Verify that the L/R needle deflects 5 dots to the right, the T/F flag displays a full FROM, the GS UP/DN needle deflects full down to the bottom bar and the GS Flag retracts fully from view.

b) Reverse the Meter (+) and (-) leads at the power supply and verify that the GS Flag is in full view, the L/R needle deflects 5 dots to the left, the T/F flag displays a full "TO", the GS UP/DN needle deflects full "UP" to the top bar.

C. MARKER BEACON LAMP TEST

1. Touch the Marker Common lead to the positive terminal (5.5 Vdc) of the power supply and verify that the White, Amber and Blue marker lamps illuminate.

D. FINAL VOR-ILS INDICATOR CALIBRATION

1. VOR/LOC CALIBRATION

The companion NAV converter, either a MK-12D, NS801 RNAV or NAV-824/825, must be calibrated with the VOR/LOC section of the IDME-891 display. The NAV converters VOR zero set and LOC zero set pots must be reset. Consult the NAV units maintenance manual for details. After VOR/LOC rezeroing, perform system specification check, as outlined in the maintenance manual.

2.2.2.3 Continued

2. GS INDICATOR CALIBRATION
The companion GS receiver/converter, either a MK-12D, NAV-825 or UGR-2A 2/5, must be calibrated with the GS indicator. The GS converters zero set pot must be reset. Consult the GS receiver's maintenance manual for details. After GS rezeroing, perform system specification, check as outlined in the maintenance manual.

2.3 ELECTRICAL INSTALLATION

The following subsections present the necessary technical information in order to plan an electrical installation. Refer to Figure 2-2, the external interconnect diagram.

2.3.1 PRIMARY POWER REQUIREMENT

The IDME-891 accepts either 14 or 28 Vdc for its primary power requirement; therefore, **NO** voltage converter is required for 28 volt aircraft electrical systems. The current draw, less indicator pilot lamps, is 0.6 amperes at 13.75 Vdc, and 0.3 amperes at 27.5 Vdc.

Primary power is applied to the rear connector at pins J301-7 and J302-26.

2.3.2 FUSE/CIRCUIT BREAKER REQUIREMENT

A thermal resettable circuit breaker or fuse must be provided by the installing agency and connected between the IDME-891 and the aircraft power bus.

For both 14 or 28 Vdc aircraft electrical systems, the circuit breaker or slow blow fuse rating required is 1.0 ampere.

2.3.3 PRIMARY GROUND REQUIREMENT

The IDME-891 has four ground connections: J301-33, J301-34, J301-35 and the rear panel support stud.

Pins J301-34 and J301-35 are the system ground terminals and are to be connected to the airframe ground.

J301-33 is a spare ground.

2.3.4 INDICATOR PILOT LAMPS

Indicator pilot lamp current draw is 0.32 amperes at either 13.75 or 27.5 Vdc.

For 14 volt electrical systems, connect P301-21 to the aircraft dimmer and ground P301-22. For 28 volt systems connect J301-22 to the aircraft dimmer.

2.3.5 IDME-891 TO NAV CONVERTER COMPATIBILITY

The VOR bearing selector in the IDME-891 Indicator head is a wire-wound potentiometer. It is only compatible with the NAV converters found in the Narco MK-12D, NAV-824/825 or NS-801 RNAV. Refer to Figure 2-2A for interconnect wiring diagram.

2.3.6 IDME-891 TO GLIDESLOPE RECEIVER COMPATIBILITY

The glideslope indicator section of the IDME-891 indicator head provides a standard 150-0-150 ua/1000 ohm UP/DOWN meter movement and a 250 ua/1000 ohm glideslope warning flag. One terminal of the GS flag is grounded internally.

Compatible Narco glideslope receivers are the NAV-825, MK-12D with glideslope, NS-801 RNAV and UGR-2A 2/5 with 2-out-of-5 remote channeling.

The UGR-2, UGR-2A and UGR-3 glideslope receivers are **NOT** compatible as they do not have 2/5 remote channeling capability. Refer to Figures 2-2A, -2B for interconnect wiring diagram.

2.3.7 IDME-891 REMOTE CHANNELING

The DME receiver in the IDME-891 must be remotely channeled by a NAV receiver capable of providing an ARINC 2/5 channeling code.

Table 2.1 lists the IDME-891 channeling code. Refer to Figures 2, 2-2A for interconnect diagrams.

2.3.8 IDENT AUDIO

The IDME-891 does **NOT** have an Ident audio volume control; therefore, a panel mounted switch is recommended to control the audio. The Ident audio consists of 5V pulses (72 usec wide) at a 1350 PRF. Because standard audio measuring techniques are not applicable for pulsed audio, the two outputs available are listed as "high" and "low" impedance. J301-10 (high impedance: 47K) is intended as a COM Aux Audio input for systems **NOT** using an audio/amplifier switching panel.
J301-29 (low impedance: 4.7K) is intended for the CP-136 audio panel. Either audio level may be shifted, if required, by changing the value of R341 (4.7K low Z) or R342 (47K Hi Z). Refer to Figures 2-2, 2-2A, 2-2B.

2.3.9 IDME-891 TO RNAV CAPABILITY

The IDME-891 is compatible with two Narco area navigation systems, the RNAV-860 and NS-801. When interfacing with the RNAV-860, the microprocessor in the IDME-891 **MUST** be replaced with a new microprocessor (Part No. 74243-0001) combined with an E Prom. Consult factory for details. No IDME-891 modification is required for an NS-801 interface. Refer to Figure 2-2A.

2.3.10 IDME-891 TO MARKER BEACON RECEIVER COMPATIBILITY

Compatible with the IDME-891 are the CP-136M and MKR-101R marker beacon receivers. Refer to Figures 2-2A, -2B.

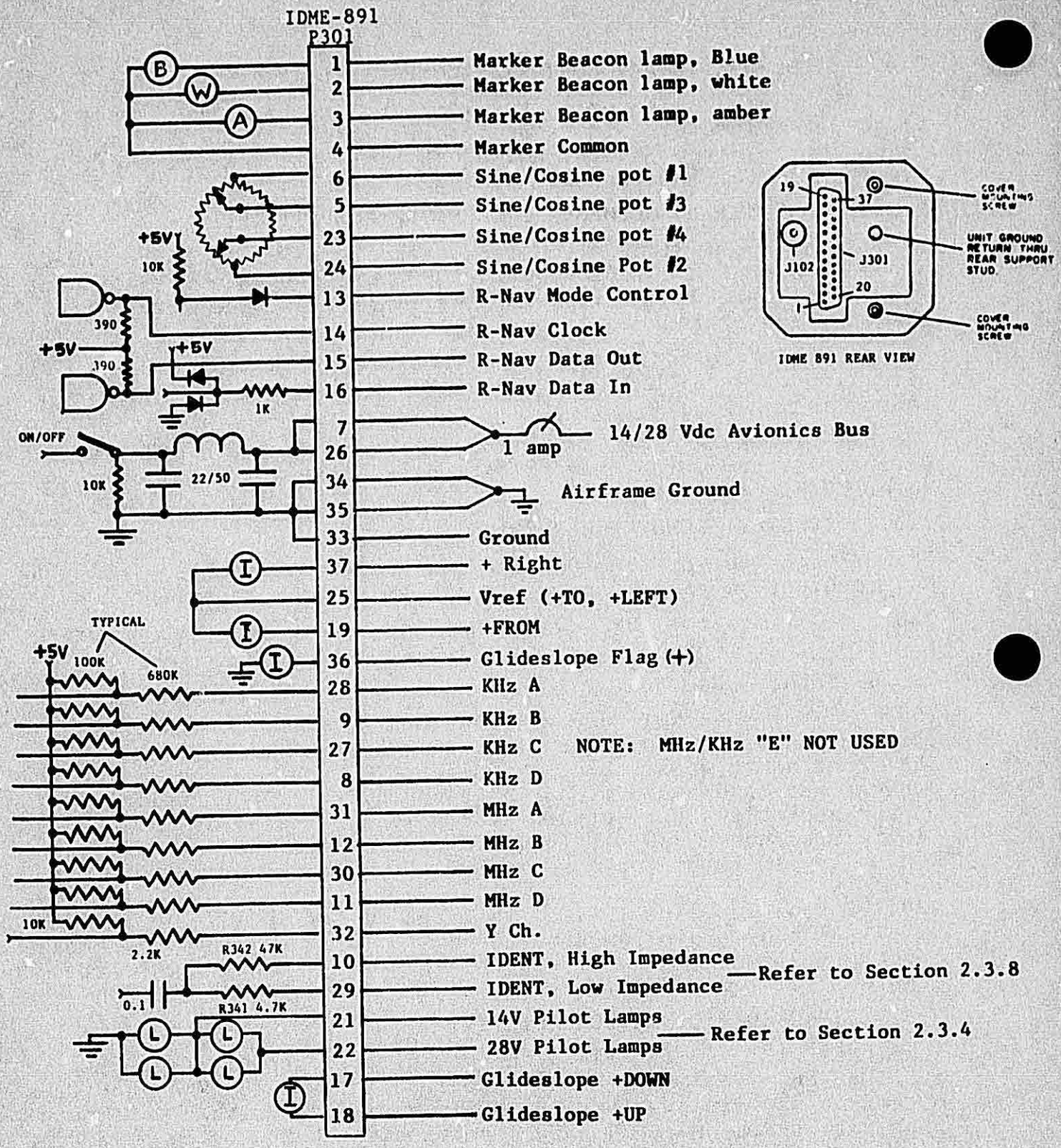


FIGURE 2-2 IDME-891 REAR CONNECTOR P301 CONNECTIONS

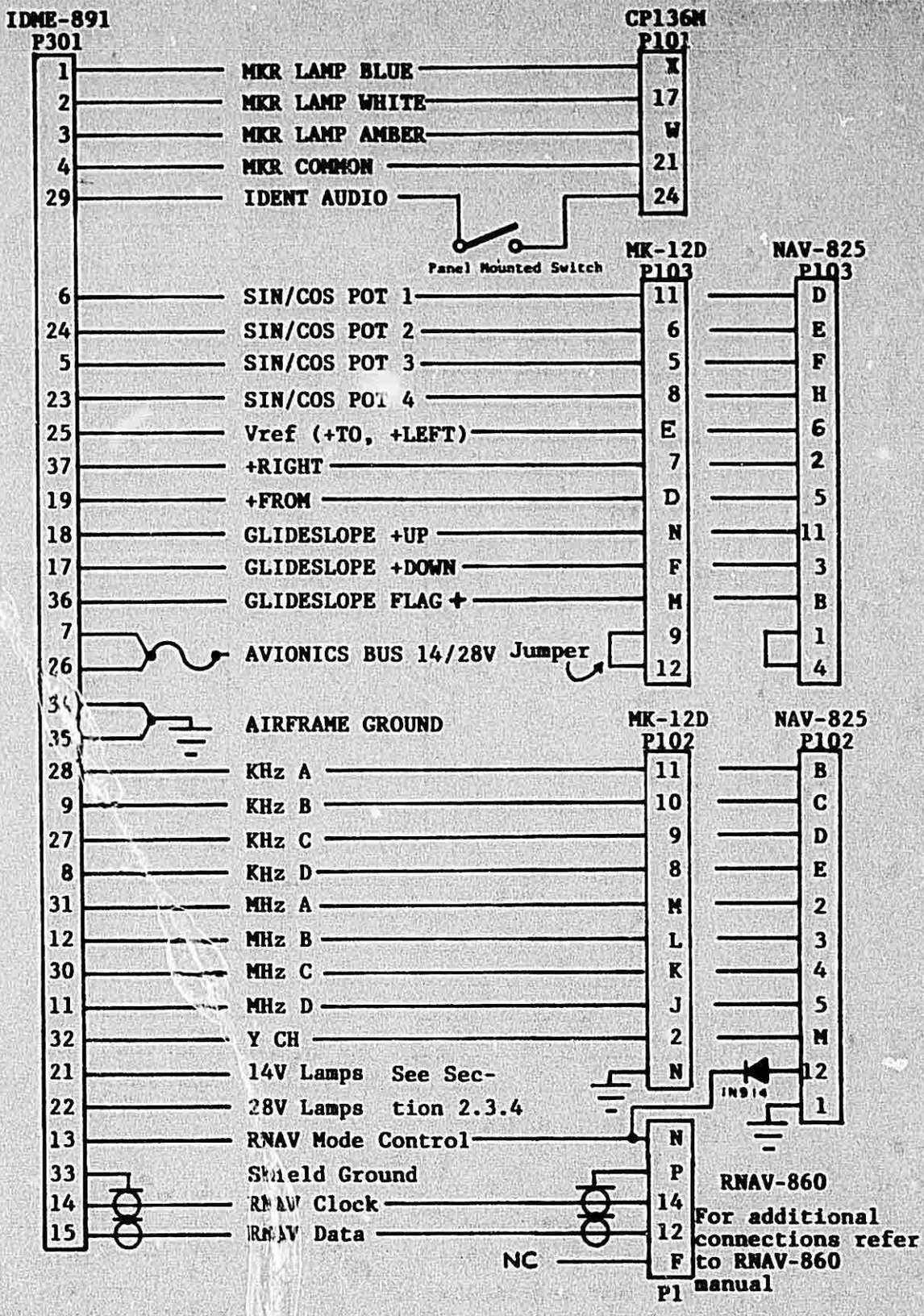
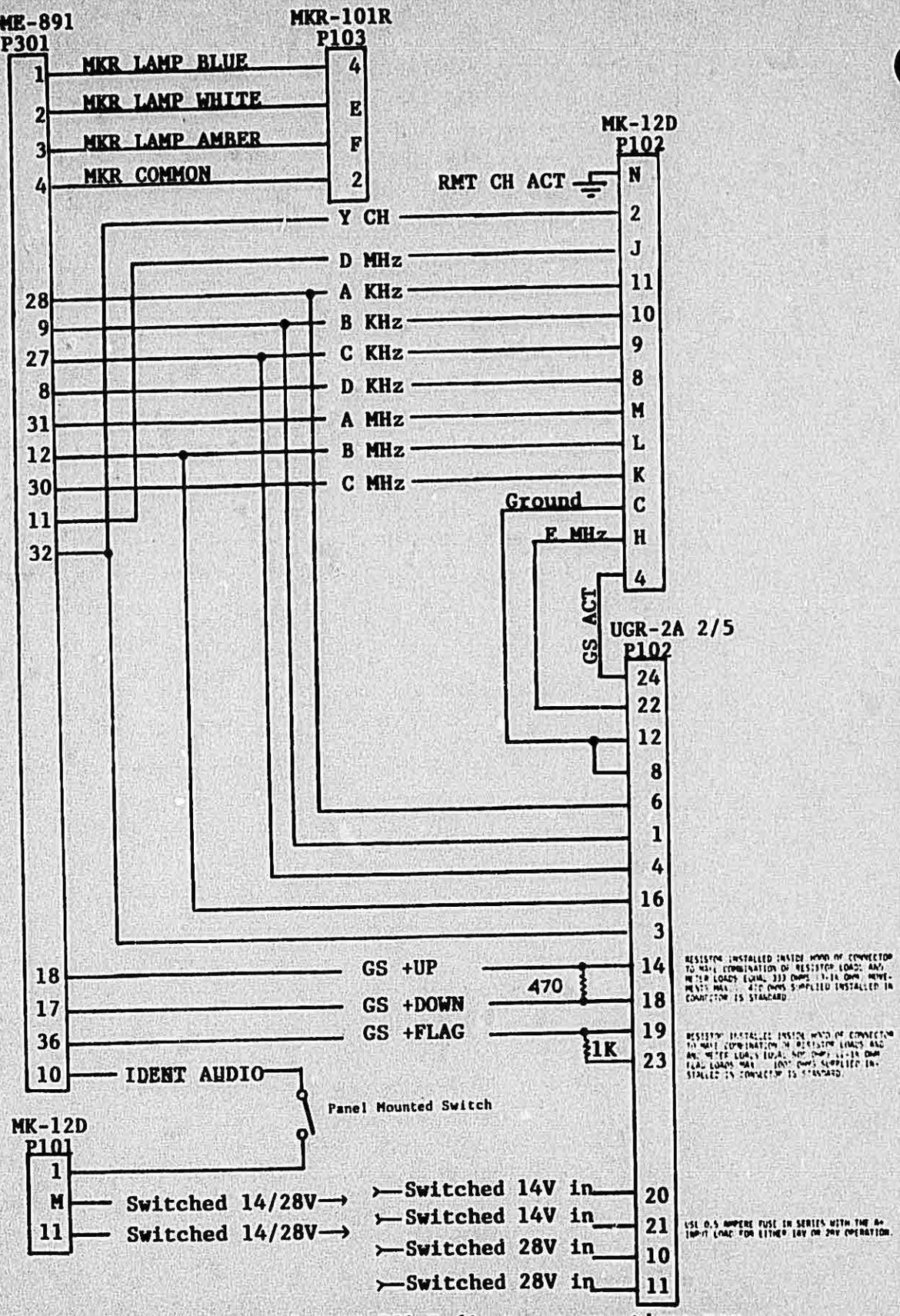


FIGURE 2-2A IDME-891 to CP-136M-RNAV-860-MK-12D or NAV-825 INTERCONNECT WIRING



NOTE: For additional IDME-891 Indicator connections see Figures 2-2/2-2A. For pilot lamp connections see Section 2.3.4.

FIGURE 2-2B IDME-891 to MK-12D wo/GS-UGR2A 2/5-MKR-101R INTERCONNECT WIRING

2.3.11 INTERCONNECT CABLE FABRICATION (P301)

Figure 2-2 lists the connections to P301. P301 is assembled as shown in Figure 2-3. While constructin the cable, be sure to pass wires through the hood before inserting pins into the connector.

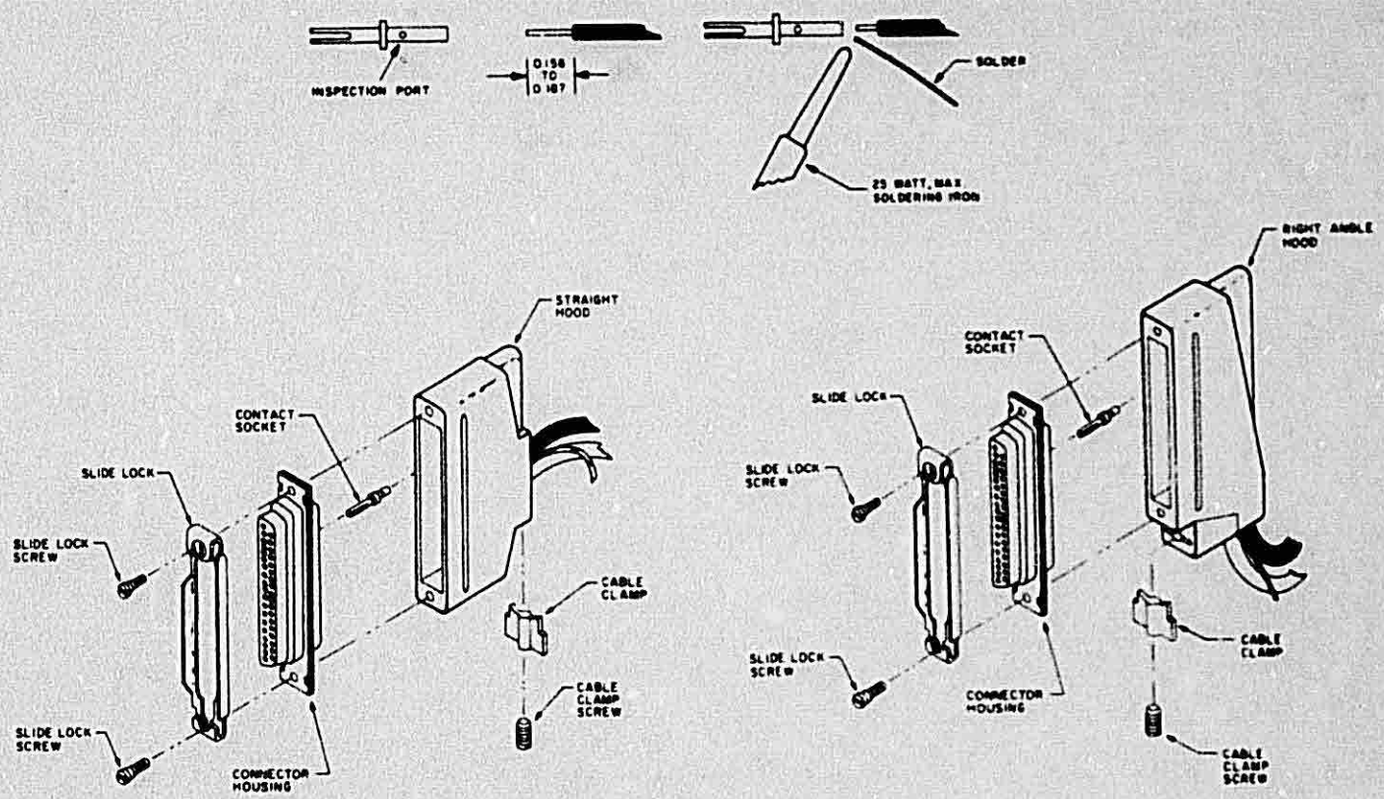


FIGURE 2-3 P301 ASSEMBLY

Connector Assembly Procedure (Solder)

NOTE: Crimping tools are available from ITT Cannon, if desired.

1. Strip wire as shown in Figure 2-3. Maximum wire size is No. 20AWG.
2. Tin exposed lead. Be sure no individual wire strands are free to cause shorts when connector is assembled.
3. Insert lead into connector pin until lead is visible at inspection port.
4. Heat pin and apply solder as shown until solder wicks into pin cavity and becomes visible through inspection port. Be careful not to overheat pin or melt insulation on wire.
5. Pass pin through hood and insert pin in connector until a "click" is heard or felt; exert a slight pull on the wire to assure pin seating.

2.3.11 Continued

6. During final assembly:
   a) Inspect all wires for individual strands of wire shorting to adjacent terminals.
   b) Ease hood into place; do not force.

Connector P301 incorporates a "slide lock" mechanism. Before installing the connector, move the slide to position the slide's longer tab away from the connector, mate J301 and P301, then push slide to lock connector to IDME unit. To remove P301 from the IDME, by feel, determine which end of the slide extends beyond the connector body, press this end toward the connector until it is flush, then remove the connector.

2.3.12 ANTENNA CABLE (P102)

A ten foot DME low loss antenna cable and connectors are supplied in the Installation Kit.

The cable run should be as direct as possible, having bend radiuses of 6 inches, minimum. In close areas a BNC 90° Adapter may be utilized to clear control cables in the vicinity of the antenna.

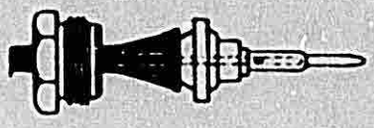
ANTENNA CABLE LOSS SHOULD BE KEPT AS LOW AS POSSIBLE. The length and type of cable is critical as the MAXIMUM cable loss should not exceed 1-1/2 dB.

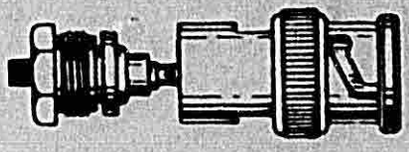
KEEP THE CABLE AS SHORT AS POSSIBLE AND CUT OFF EXCESS LENGTHS! If it is necessary to run the antenna cable some distance or should the cable be changed, refer to the following examples and take note of their limitations.

Cable Type	dB loss per 100 ft. @ 1000 MHz	Preferred Length 1 dB or less	Maximum length 1-1/2 dB loss
RG 58 A/U	22. (.22 dB per ft)	4-1/2 ft.	6 ft.
RG 29 /U	17. (.17 dB per ft)	6 ft.	8 ft.
RG 223 /U (90092)Narco	16.4 (.164 dB per ft)	6 ft.	9 ft.
RG 54 A/U	11.5 (.115 dB per ft)	8-3/4 ft.	11 ft.
Narco(90072)	10. MAX (.10 dB per ft)	10 ft.	15 ft.
RG 8 /U	8.5 (.085 dB per ft)	11-3/4 ft.	17 ft.

Figure 2-4 shows the proper method of connecting the BNC connectors to the antenna cable.

2.3.12 Continued





1. Take one clean square cut through cable insulation, braid and dielectric, exposing ¼" of conductor. Slip nut onto cable.

2. Insert conductor into tapered, self-clamping sleeve and contact sub-assembly, force edge of sleeve between dielectric and braid until insulation rides well onto taper. Solder conductor to contact at solder hole.

3. Fit contact sub-assembly into connector body, screw nut into body, binding insulation and braid tightly against tapered sleeve, thus forming a strong, weatherproof connection.

Courtesy of Bendix Corp.

All illustrations enlarged for clarity

FIGURE 2-4 BNC CABLE CONNECTOR

2.4 MECHANICAL INSTALLATION

This section provides the mechanical installation steps for mounting the antenna and IDME-891.

2.4.1 UDA-3 ANTENNA MOUNTING

The Blade antenna, type UDA-3, is used for both receiving and transmitting by the DME. This antenna should be mounted on the bottom surface of the aircraft and located so that it is in the vertical position when the aircraft is in a level flight attitude. The mounting surface should be metal, electrically grounded, and extend at least 6″ in all directions from the antenna connector. A three (3) foot minimum separation from other antennas, particularly transponders should be maintained.

Avoid mounting the antenna in the vicinity of aircraft protrusions as this is likely to create some radiation "shadowing" with a resultant loss in signal strength from both transmitted and reply signals.

If this antenna is to be used on non-metallic aircraft skin, a ground plane at least 6″ in diameter must be provided. This could be as simple as aluminum foil cemented inside a wood or fiberglass skin, or a doubler plate on a fabric-covered aircraft. Such a ground plane should be either well bonded to the airframe, or well insulated from it, to prevent erratic operation.

A doubler plate will be needed for an airworthy installation on most aircraft. Check the airworthiness regulations of the country of aircraft registry for acceptable mounting methods. Figure 2-5 is removable for a drilling template.

DO NOT PAINT. This antenna may not be coated with any paint or other finish.

2.4.2 IDME-891 MECHANICAL INSTALLATION

The IDME-891 is intended to be instrument panel mounted (See Figure 2-7). When mounted from behind the panel, two screws (6-32 x 7/16) and the unit's ON-OFF-DIM bushing secure the Unit (see Figure 2-6). Rear support should be supplied using the stud extending from the rear of the Unit.

Connector P301 incorporates a "slide's lock" mechanism. Before installing the connector, move the slide to position the slide's longer tab away from the connector, mate J301 and P301, then push slide to lock connector to Unit. To remove P301 from the Unit, by feel, determine which end of the slide extends beyond the connector body, press this end toward the connector until it is flush, then remove the connector.

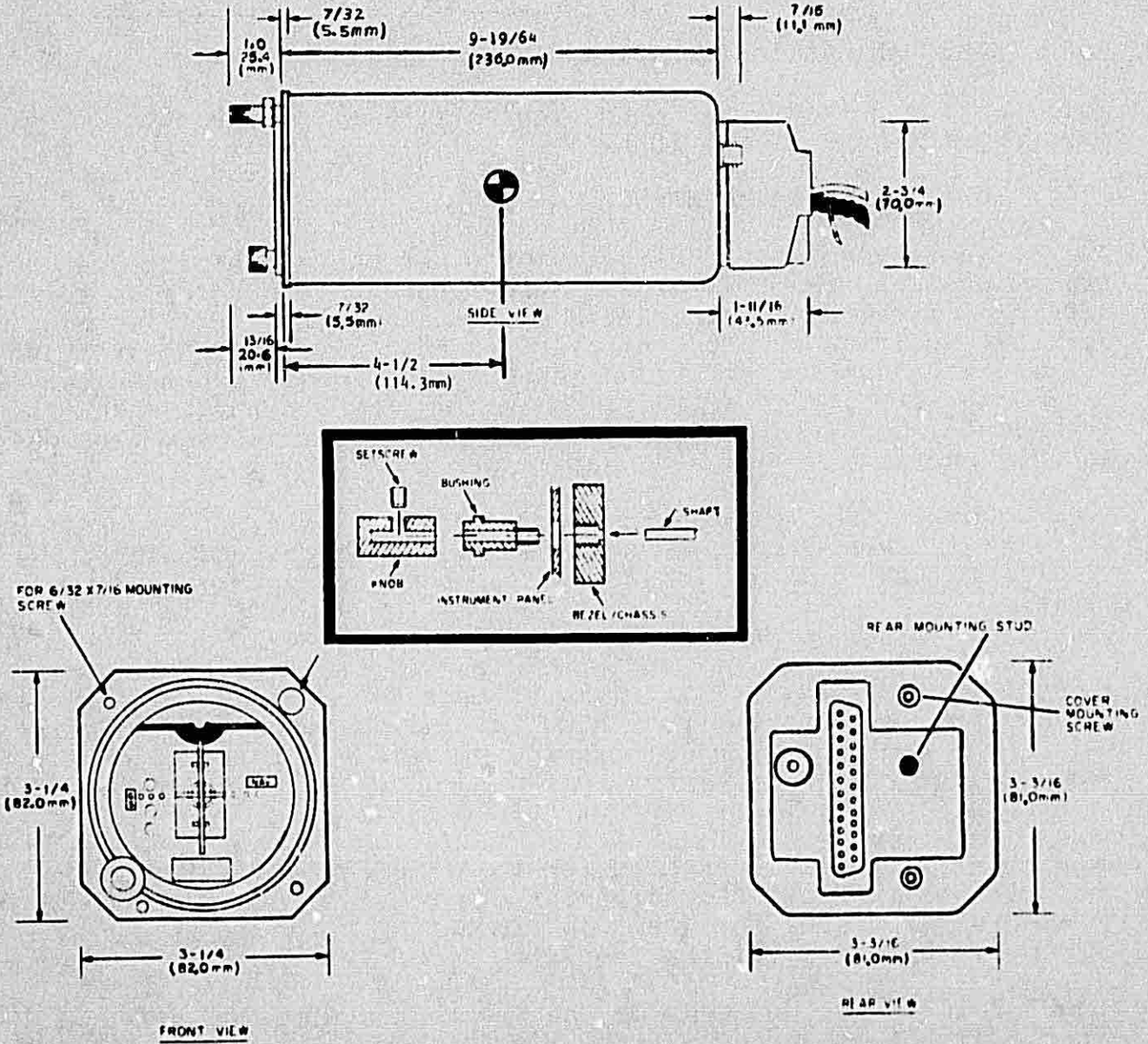


FIGURE 2-6 IDME-891 PANEL MOUNTING

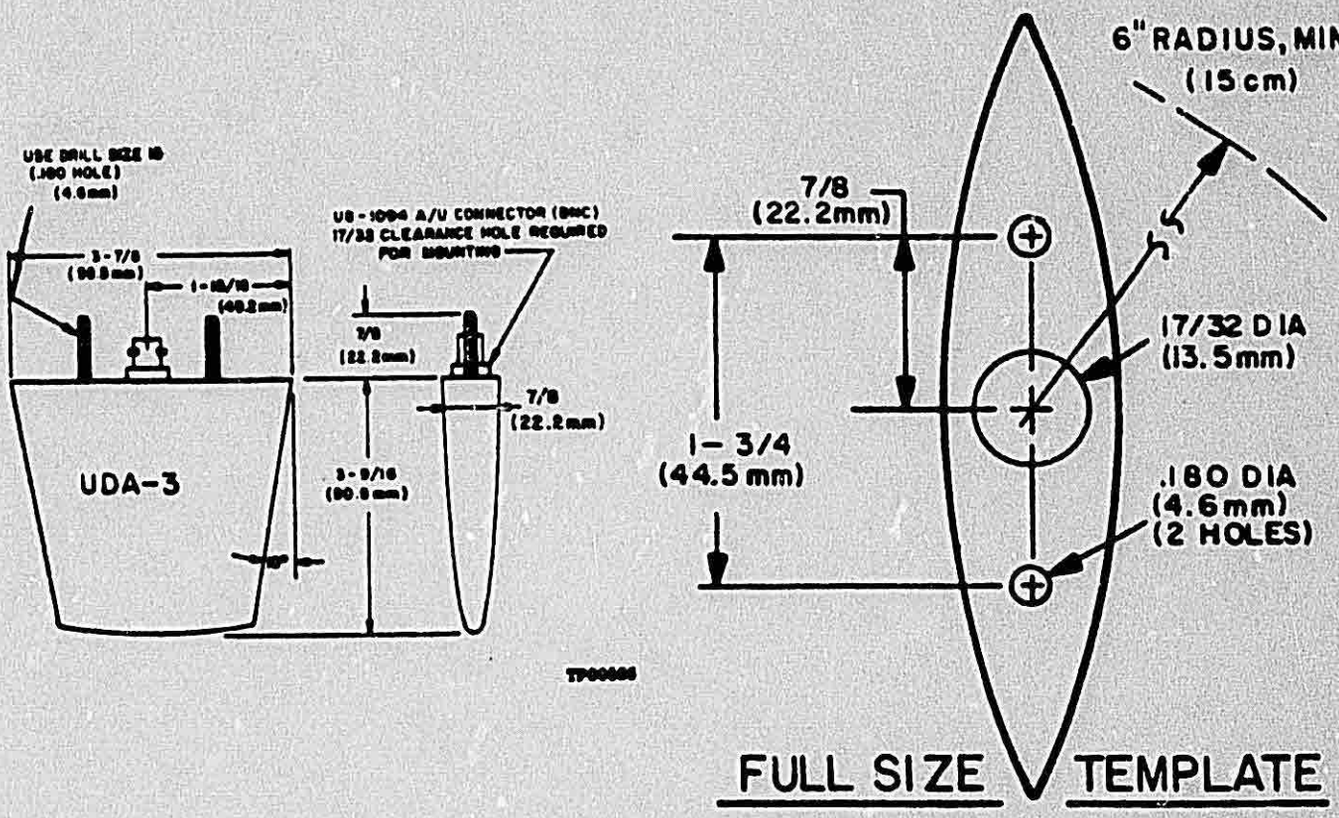


FIGURE 2-5 UDA-3 ANTENNA

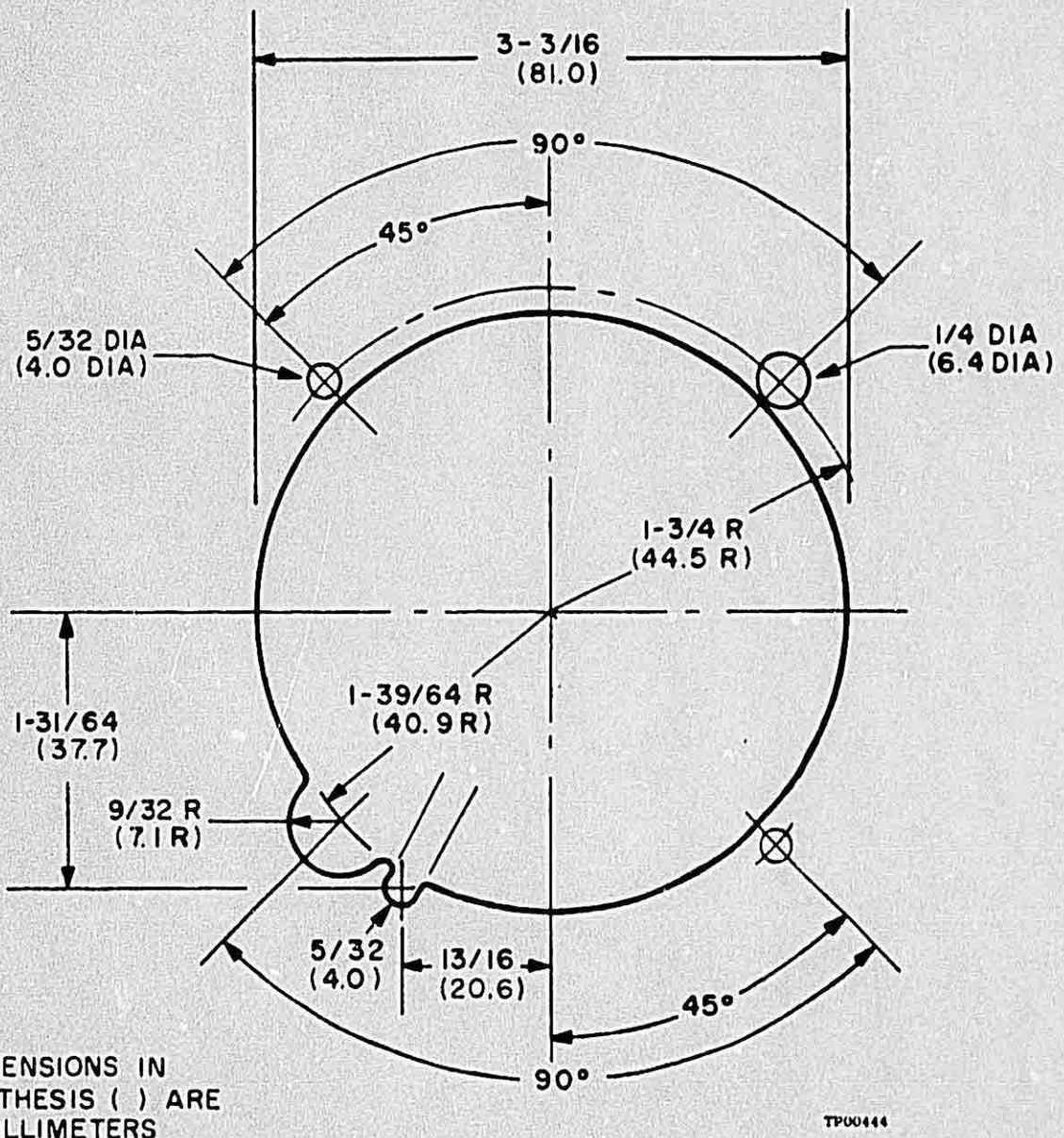


FIGURE 2-7. MOUNTING TEMPLATE, REAR MOUNT

2.5 POST INSTALLATION CHECK

Both the PreFlight check and Flight check are recommended after installation and major repair.

2.5.1 DME PREFLIGHT CHECK

Use a Ramp Test Signal Generator or a local station of known distance for the DME PreFlight check.

1. Channel NAV unit to proper DME frequency.
2. Distance (NM) should be in agreement with that set in the generator or that of the actual station (accuracy ±.1 NM).
3. Check ground speed if using a generator.
4. Check that audio Ident tone is present.
5. If using a ramp test signal generator, check the DME for operation of the NAV unit's remote channeling capability.

NOTE: Some Test Generators do not simulate actual signals and may not operate the DME.

2.5.2 VOR-ILS PREFLIGHT TESTS

For this series of in-aircraft tests, the aircraft's engines, rotating beacon, electrical and avionics equipment should be operating. Note any abnormal interaction or interference (ignition or rotating beacon noise, abnormal meter deflection, compass deviation, etc.) observed during these tests.

The following procedure requires ramp type test equipment such as that offered by Tel-Instrument Corp. or IFR Inc.

A. GENERAL

1. Set NAV Receiver to a VOR frequency.
2. Rotate the VOL-IDENT control clockwise until NAV Receiver noise is heard in the speaker and headphones. Note presence of NAV and GS warning flags and centered Left-Right and Up-Down needles.
3. Modulate test equipment 30% with 1020 Hz.
4. Pull VOL-IDENT knob and note presence of adequate volume level. Depress VOL-IDENT knob and note decrease in volume level.

B. VOR

1. Set test equipment and NAV Receiver to a VOR frequency. Modulation should be a composite VOR signal.
2. Set test equipment and NAV Receiver OBS to 0° course.
   Spec: Left-Right needle must center within ±1.5° with a TO Flag. For VOR "zero set" adjustment, consult NAV maintenance manual.
3. Turn OBS knob to first 10° then 350°.
   Spec: Left-Right needle should deflect full scale (5 dots).

2.5.2 Continued

4. Check remaining three cardinal points (90°, 180° and 270°).
   Spec: Left-Right needle must center within 1.5° with a TO Flag.

C. LOC

1. Set test equipment and NAV Receiver to a LOC frequency. Modulation should be a standard LOC centering signal.
   Spec: Centering, ±1 needle width with a TO flag.
   For LOC "zero set" adjustment consult NAV maintenance manual.
2. Change modulation to 4 dB ddm left then right.
   Spec: deflection, 3 dots, ±1 needle width.
3. Remove modulation or decrease test equipment RF output to minimum.
   Spec: LOC warning flag shall be full.

D. GLIDESLOPE

1. Set test equipment and NAV Receiver to a GS frequency. Modulation should be a standard GS centering signal.
   Spec: Centering, ±1 needle width with a GS Flag retracted.
2. Change modulation to 2 dB ddm Up then Down.
   Spec: Deflection, 1.5 dots, ±1 needle width with GS Flag retracted.
3. Remove modulation or decrease test equipment RF output to minimum.
   Spec: GS warning flag shall be fully in view.

E. MARKER BEACON LAMPS

1. Depress marker lamp test on CP-136M or MKR-101R.
   Spec: All three lamps must light.
2. Modulate Marker test equipment 90% with 3,000 Hz.
   Spec: White lamp must light.
3. Change modulation frequency to 400 Hz then 1300 Hz.
   Spec: First the blue than the amber lamp must light.
4. Check marker audio for adequate volume.

2.5.3 VOR-ILS FLIGHT TEST

A flight test is recommended to perform the following checks and adjustments.

A. Check all avionics under actual operating conditions for abnormal indications (ignition noise, audio distortion at in-flight volume settings, rotating beacon noise, interference between avionics equipments, etc.)
B. Proportion audio volume levels.
C. Look for variations in performance due to various landing gear and flight control surface configurations.

All of these tests must be performed at an ILS facility, on an airway, or in an area where the ground station signal quality and strength has been verified.

VOR

A. Flying at an altitude of 6,000 feet above ground level (AGL) channel the NAV Receiver to a VOR facility 50 nm away.
    1. Check course accuracy, warning flag indication, and left-right needle sensing.
    2. Check the antenna pattern by flying the aircraft in a 10° bank completing a 360° turn: the warning flag should remain out of view throughout the turn and audio should remain intelligible.
B. Flying at an altitude of 6,000 feet AGL, channel the NAV Receiver to a VOR facility 10 nm away and fly inbound.
    1. Check course width (±10° of selected radial).
    2. Observe the VOR warning flag while approaching, passing over, and flying outbound: TO-FROM indicator shall indicate correctly and the warning flag must not be observed except when passing directly over the station.
C. Flying at an altitude of 6,000 feet AGL, channel the NAV Receiver to a VOR facility 25 nm away and fly inbound.
    1. Operate the communication transceiver: VOR left-right indicator transient deviations should not exceed 2 dots and steady state errors should not exceed 0.5 dot.
D. Engage autopilot and couple to VOR. Check tracking and intercept performance.

2.5.3 Continued

LOC, GS and MARKER BEACON

Flying at an altitude of 3,000 feet AGL, channel the NAV Receiver to a LOC frequency and fly inbound to intercept ILS.

1. From point of intercept to termination of test, neither LOC or GS warning flags should appear.
2. Establish glide path and fly the ILS approach: request ground control confirmation of on-glide path condition.
3. While flying the ILS approach, confirm the operation of the white, amber and blue marker beacon lamps as each marker is passed.
4. While on-glide path, maneuver aircraft through normal pitch and roll altitudes: Left-right and up-down indicators should perform normally and a warning flag should not be visible at any time.
5. Engage autopilot and fly a coupled ILS approach.

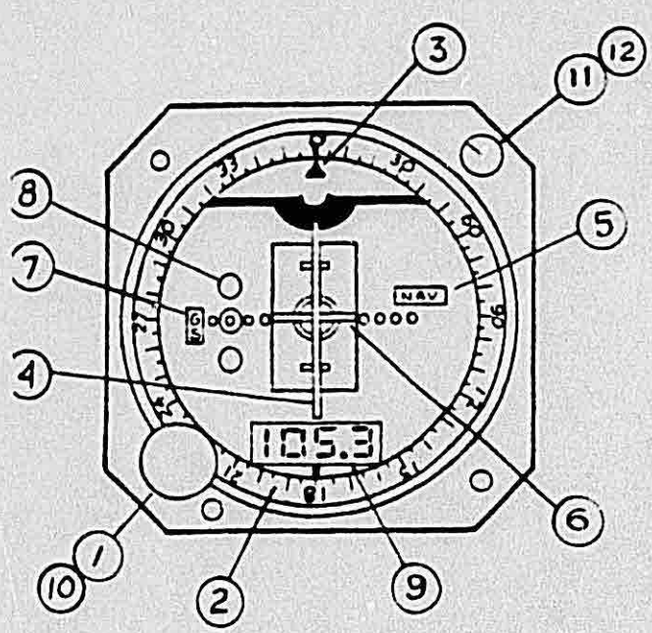
2.5.4 DME FLIGHT TEST

1. At 6,000 feet altitude, range 50 NM, check that there are no dropouts during a flat 360° turn.
2. High Angle Check: While flying at an altitude of 6,000 to 10,000 feet (above the station's elevation) and from a distance of 10 NM, track inbound to the station and then track the reciprocal course. In each pass check the accuracy at the critical points....over the station and at the 10 NM point.
3. Orbit Approach: At a distance of 10 DME miles fly an orbit for one (1) minute. There shall be no dropouts. Repeat this flight in the opposite direction.
4. Electromagnetic Compatability: The DME should not cause the performance of other systems aboard the aircraft to be degraded nor should the DME be adversely affected by other onboard equipment. This can be checked by turning such equipments ON and OFF one by one and listening and viewing the resultant action. There should be no reactions.

3.1 INTRODUCTION TO OPERATION

Operation of the IDME-891 remote channeled DME with VOR-ILS indicator is described here only to the extent of making the electrical tests necessary to confirm proper operation. Operation of the unit, as applied to navigating an aircraft, is not covered in this manual.

3.2 IDME-891 FRONT PANEL DESCRIPTION



1. VOR Bearing Select Knob.
2. VOR Bearing Dial.
3. VOR Bearing Index.
4. VOR/LOC Indicator.
5. VOR TO/FROM/Warning Flag.
6. Glideslope Indicator
7. Glideslope Warning Flag
8. Marker Beacon Lamps
9. DME L.E.D. Display
10. Push Knob for DME Groundspeed
11. Power "ON-OFF" Switch
12. DME L.E.D Display Dimmer Control

FIGURE 3-1 IDME-891 FRONT PANEL

3.3 VOR BEARING SELECTION CONTROL

The VOR bearing selection control is the knob at the lower left of the indicator. The selected bearing is shown on a moving VOR bearing dial under an index at the top of the indicator. The reciprocal bearing appears under an index, at the bottom of the indicator.

3.4 INDICATORS

3.4.1 VOR/LOC DEVIATION INDICATOR

For VOR Steering, the vertically oriented Indicator moves left or right to indicate selected VOR bearing relative to actual aircraft heading. When the indicator is centered, an ON-course condition exists.

For LOC Steering, the Indicator moves left or right to locate the lateral centering component of an ILS glide path system relative to actual aircraft heading.

3.4.2 GLIDESLOPE DEVIATION INDICATOR

The horizontally oriented Indicator moves up or down to locate the vertical centering component of an ILS glidepath system relative to the actual aircraft heading.

The required glidepath of the aircraft is obtained only when the GS and LOC Deviation Indicators are crossed and centered within the small circle.

3.5 WARNING FLAGS

3.5.1 NAV FLAG (TO/FROM)

A Red NAV Flag (Red OFF) alerts the pilot to either a loss of VOR/LOC signal or inadequate signal level. When a valid signal is received, either a TO or FROM Flag will appear depending on whether the selected course will take the aircraft to or from the station.

3.5.2 GLIDESLOPE FLAG

A Red GS Flag (Red OFF) alerts the pilot to either a loss of signal or inadequate signal level.

3.6 MARKER BEACON LAMPS

The marker beacon lamps are used to mark locations on the ILS system, and to mark selected airways points. The ILS Outer Marker is the BLUE lamp, the Inner Marker is the AMBER Lamp and the "Z" or airways marker is the WHITE lamp.

3.7 OPERATING PROCEDURES

3.7.1 POWER SWITCHING (ON/OFF)

The IDME-891 is turned "OFF" by the extreme CCW position of the Dimmer control. CW rotation beyond the detent turns the unit "ON".

3.7.2 VOR CHANNEL SELECTION

When the IDME-891 is properly installed and connected, the associated NAV and/or GS receiver must be tuned to the desired VOR or GS/LOC channel.

3.7.3 VOR OPERATION

With the NAV receiver properly tuned and a VOR bearing, TO or FROM, selected on the VOR Generator, rotate the VOR Bearing Selector knob until the Left-Right Indicator is centered. If a valid signal is received, the NAV Flag should retract and a TO or FROM Flag should appear. The magnetic bearing TO or FROM the simulated VOR station is then read under the index at the top of the VOR bearing dial.

3.7.4 LOCALIZER OPERATION

With the NAV receiver tuned to a localizer channel and a LOC centering signal set on the VOR generator, the Red NAV Flag should retract to the TO position if a valid signal is received and the Left-Right Indicator should center. When the LOC centering signal at the VOR Generator is moved to favor the 90 Hz component of the composite signal, the Left-Right Indicator will move to the right. Favoring the 150 Hz component will move the indicator to the left.

3.7.5 GLIDESLOPE OPERATION

Glideslope transmitters are paired with localizer transmitters in the ILS system. Glideslopes oeprate at UHF frequencies. A glideslope frequency is assigned to each localizer frequency. Most glideslope receivers are remotely tuned by the NAV receiver.

With the glideslope receiver properly tuned and a GS centering signal set on the VOR/GS generator, if a valid signal is received, the Red GS Flag will retract and the GS indicator should go to the center position. When the GS centering signal at the VOR/GS generator is moved to favor the 150 Hz component of the composite signal, the GS indicator will move UP. Favoring the 90 Hz component will move the GS indicator down.

3.8 DME OPERATION

3.8.1 DME CHANNEL SELECTION

The IDME-891 has **NO** DME tuning controls as it is remotely channeled by its companion NAV receiver (MK-12D or NAV-824/825). When the IDME-891 is properly installed and connected, the associated NAV unit must be tuned to the desired DME channel.

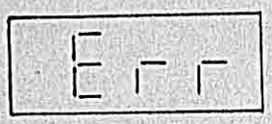
3.8.2 DME LIGHT EMITTING DIODE (L.E.D.) DISPLAY

The DME readout is a 4-digit 7-segment high intensity L.E.D. display. Range in nautical miles to the nearest 0.1 nm is normally displayed when locked-on to the set ground station. A fault condition is indicated when "BARS" are displayed.

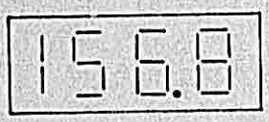
TYPES OF DISPLAY INDICATIONS

FAULT - Indicates an unuseable signal or circuit defect.

FREQUENCY - Immediately following a remote channel selection, push in the OBS knob and for 5 seconds, the MHz frequency will be displayed. The KHz frequency is not displayed. After 5 seconds, the display will indicate the preset velocity (120 kts).



ERROR - When the OBS knob is pushed in and "Err" is displayed, this indicates a false ARINC channeling code.



RANGE - The display normally indicates range in nautical miles.

VELOCITY - When the OBS knob is pushed in, the display indicates velocity in nautical miles per hour.

3.8.3 DME GROUNDSPEED SELECTION

To read DME groundspeed in the L.E.D. display, the VOR Bearing Select Knob must be depressed and held depressed. The groundspeed is given in knots to the nearest whole digit. Accuracy is ±5% after 5 minutes stabilization of the initial lock-on. When the Bearing Select Knob is released, the display reverts back to DME range.

Displayed Time-to-Station (TTS) is **NOT** available in the IDME-891 system.

3.8.4 DME L.E.D. DISPLAY DIMMING CONTROL

The intensity of the L.E.D. display is manually controlled by the Dimmer Knob located at the upper right of the Indicator. The dimmer pot is part of the unit's "ON-OFF" switch. CW knob rotation dims the display while CCW rotation increases brightness.

NARCO AVIONICS IDME-891

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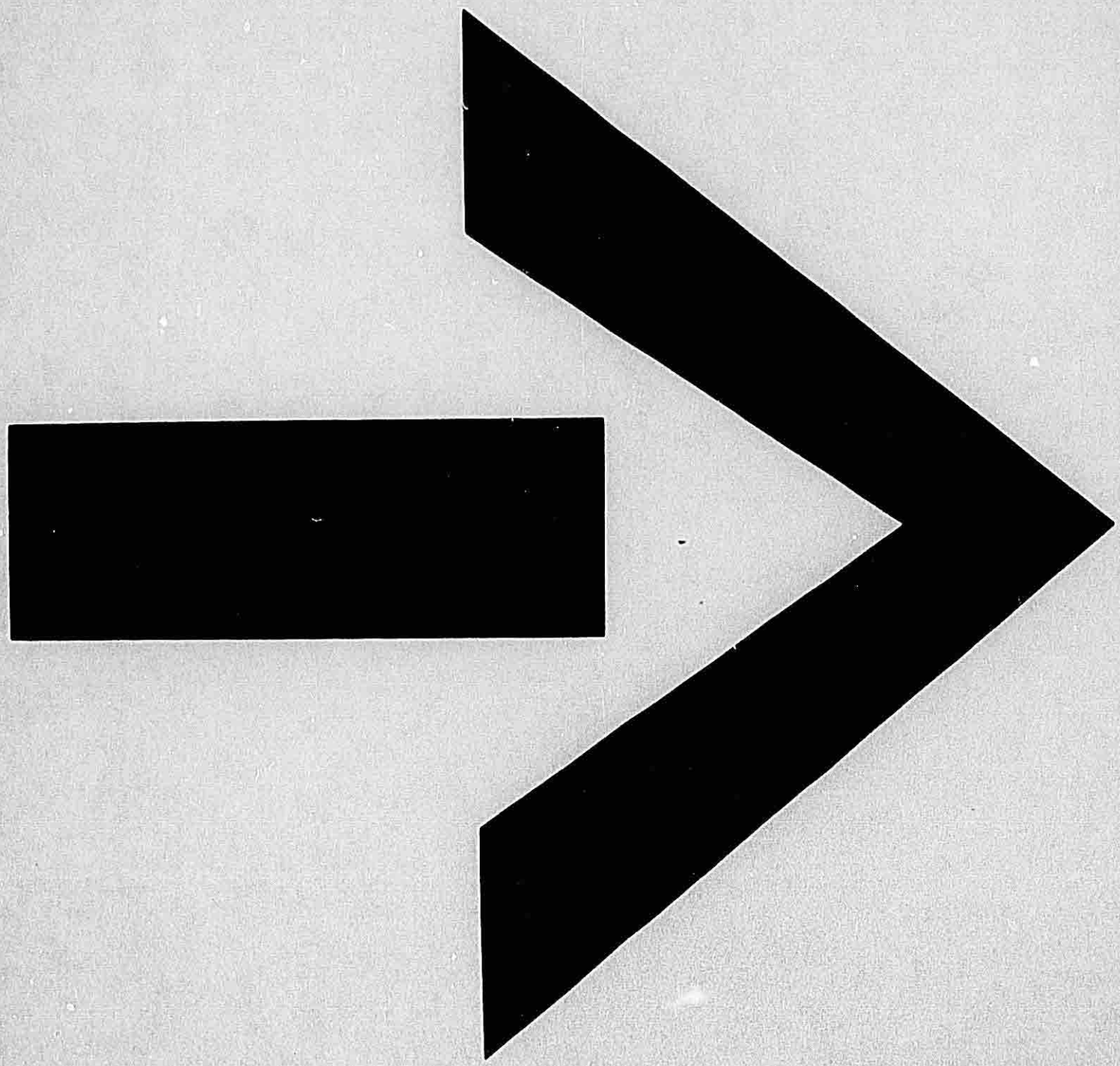


4-1 BASIC DME GROUND/AIRBORNE OPERATION

A full cycle of DME operation includes the transmission of a radio signal from the aircraft to the ground station and reply from the ground station to the aircraft. The time required for this process is determined by the distance between the aircraft and ground station. The aircraft transmits a pair of pulses at (approximately) a 30 Hz repetation rate and the signal is received at the ground station as shown in Figure 4-1. After a fixed delay of 50 micro-seconds (us) by the ground station, it transmits a pulse pair back to the aircraft. The airborn receiver must then confirm that: the pulse pair is the result of its original transmission, measure the time taken for this round trip radio signal, and display the time period as distance in nautical miles. The airborne DME must take into consideration that the ground station simulates these events when not being interrogated. The ground station also takes time-out from replies to transmit its own identification (IDENT) that consists of regularly spaced pulses (dots and dashes of Morse code) that can be heard on the aircraft's audio system.

The DME is therefore an instrument that measures the time required for a radio signal to travel to and from the ground station. The time required is a function of the distance measured in nautical miles and the 50 us delay in the transmission of a reply. The radio wave requires 12.36 us to travel through one nautical mile of space and return. The DME has a resolution of 0.1 nm. The 50 us delay by the ground station is to allow the DME receiver to recover from the DME transmitter blast. This 50 us delay is the same for all DME ground station transmitters. The airborne DME compensates for this 50 us delay. The DME is capable of recognizing the correct reply, although not every interrogation gets a reply.

The DME ground station has three basic functions: retransmits any receiver signal, during "off time", generates squitter, and generates an IDENT signal. When retransmitting, this ground station reply may be in response to an interrogation from another aircraft, the DME, however, is able to disregard the other replies, recognize only the correct reply and process only this signal. If the ground station is sending IDENT or squitter, or replying to another aircraft, it will not reply to your DME interrogations.

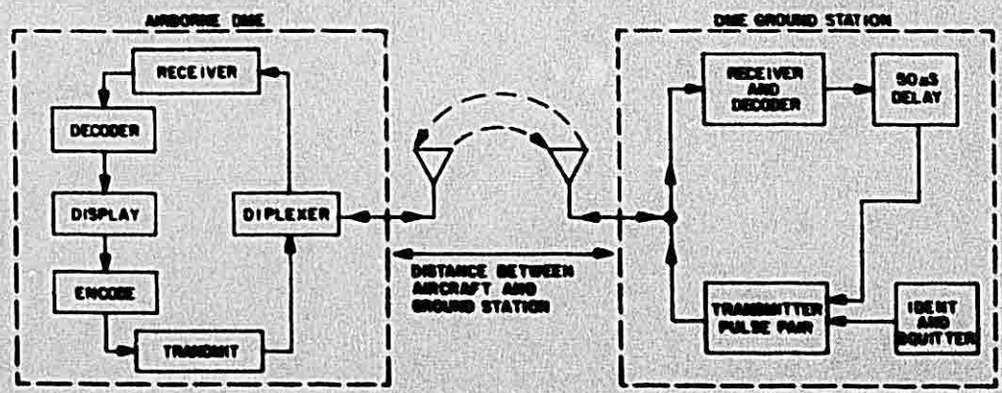


FIGURE 4-1. ELEMENTARY AIR/GROUND DME

4.2 IDME 891 AIRBORNE OPERATION

The DME transmitter operates within the frequency range of 1041 through 1150 MHz and the receiver frequencies are 978 through 1213 MHz; transmit and receive frequencies on any given channel are offset by 63 MHz, the receiver IF frequency. These operating frequencies are paired to operate with the associated OMNI channel as shown in Table 4.1. The DME channel is remotely selected by the setting of the MHz and KHz channel select switches, on a remote NAV Receiver. VOR channels 108.00 through 117.95 MHz are indicated as they are paired directly with the DME ground station located at VORTAC or VOR ground stations. The channeling lines which are ARINC 2-out-of-5, are connected directly to the search track counters as shown in Figure 4-2. The synthesizer operating frequency is 1/2 the transmit output frequency. The pulse repetition frequency (PRF) source is the microprocessor that turns on the transmitter pulse modulator at approximately 30 Hz rate.

TABLE 4.1. VOR/DME CHANNEL PAIRING AND OPERATING FREQUENCIES

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
+17X	108.00	1041	520.50	12	978	12
17Y	108.05	1041	520.50	36	1104	30
18X	108.10	1042	521.00	12	979	12
18Y	108.15	1042	521.00	36	1105	30
19X	108.20	1043	521.50	12	980	12
19Y	108.25	1043	521.50	36	1106	30
20X	108.30	1044	522.00	12	981	12
20Y	108.35	1044	522.00	36	1107	30
21X	108.40	1045	522.50	12	982	12
21Y	108.45	1045	522.50	36	1108	30
22X	108.50	1046	523.00	12	983	12
22Y	108.55	1046	523.00	36	1109	30
23X	108.60	1047	523.50	12	984	12
23Y	108.65	1047	523.50	36	1110	30
24X	108.70	1048	524.00	12	985	12
24Y	108.75	1048	524.00	36	1111	30
25X	108.80	1049	524.50	12	986	12
25Y	108.85	1049	524.50	36	1112	30
26X	108.90	1050	525.00	12	987	12
26Y	108.95	1050	525.00	36	1113	30
27X	109.00	1051	525.50	12	988	12
27Y	109.05	1051	525.50	36	1114	30
28X	109.10	1052	526.00	12	989	12
28Y	109.15	1052	526.00	36	1115	30
29X	109.20	1053	526.50	12	990	12
29Y	109.25	1053	526.50	36	1116	30
30X	109.30	1054	527.00	12	991	12
30Y	109.35	1054	527.00	36	1117	30
31X	109.40	1055	527.50	12	992	12
31Y	109.45	1055	527.50	36	1118	30
32X	109.50	1056	528.00	12	993	12
32Y	109.55	1056	528.00	36	1119	30
33X	109.60	1057	528.50	12	994	12
33Y	109.65	1057	528.50	36	1120	30
34X	109.70	1058	529.00	12	995	12
34Y	109.75	1058	529.00	36	1121	30

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
35X	109.80	1059	529.50	12	996	12
35Y	109.85	1059	529.50	36	1122	30
36X	109.90	1060	530.00	12	997	12
36Y	109.95	1060	530.00	36	1123	30
37X	110.00	1061	530.50	12	998	12
37Y	110.05	1061	530.50	36	1124	30
38X	110.10	1062	531.00	12	999	12
38Y	110.15	1062	531.00	36	1125	30
39X	110.20	1063	531.50	12	1000	12
39Y	110.25	1063	531.50	36	1126	30
40X	110.30	1064	532.00	12	1001	12
40Y	110.35	1064	532.00	36	1127	30
41X	110.40	1065	532.50	12	1002	12
41Y	110.45	1065	532.50	36	1128	30
42X	110.50	1066	533.00	12	1003	12
42Y	110.55	1066	533.00	36	1129	30
43X	110.60	1067	533.50	12	1004	12
43Y	110.65	1067	533.50	36	1130	30
44X	110.70	1068	534.00	12	1005	12
44Y	110.76	1068	534.00	36	1131	30
45X	110.80	1069	534.50	12	1006	12
45Y	110.85	1069	534.50	36	1132	30
46X	110.90	1070	535.00	12	1007	12
46Y	110.95	1070	535.00	36	1133	30
47X	111.00	1071	535.50	12	1008	12
47Y	111.05	1071	535.50	36	1134	30
48X	111.10	1072	536.00	12	1009	12
48Y	111.15	1072	536.00	36	1135	30
49X	111.20	1073	536.50	12	1010	12
49Y	111.25	1073	536.50	36	1136	30
50X	111.30	1074	537.00	12	1011	12
50Y	111.35	1074	537.00	36	1137	30
51X	111.40	1075	537.50	12	1012	12
51Y	111.45	1075	537.50	36	1138	30
52X	111.50	1076	538.00	12	1013	12
52Y	111.55	1076	538.00	36	1139	30

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
53X	111.60	1077	538.50	12	1014	12
53Y	111.65	1077	538.50	36	1140	30
54X	111.70	1078	539.00	12	1015	12
54Y	111.75	1078	539.00	36	1141	30
55X	111.80	1079	539.50	12	1016	12
55Y	111.85	1079	539.50	36	1142	30
56X	111.90	1080	540.00	12	1017	12
56Y	111.95	1080	540.00	36	1143	30
57X	112.00	1081	540.50	12	1018	12
57Y	112.05	1081	540.50	36	1144	30
58X	112.10	1082	541.00	12	1019	12
58Y	112.15	1082	541.00	36	1145	30
59X	112.20	1083	541.50	12	1020	12
59Y	112.25	1083	541.50	36	1146	30
70X	112.30	1094	547.00	12	1157	12
**70Y	112.35	1094	547.00	36	1031	30
71X	112.40	1095	547.50	12	1158	12
**71Y	112.45	1095	547.50	36	1032	30
72X	112.50	1096	548.00	12	1159	12
**72Y	112.55	1096	548.00	36	1033	30
73X	112.60	1097	548.50	12	1160	12
**73Y	112.65	1097	548.50	36	1034	30
74X	112.70	1098	549.00	12	1161	12
**74Y	112.75	1098	549.00	36	1035	30
75X	112.80	1099	549.50	12	1162	12
**75Y	112.85	1099	549.50	36	1036	30
76X	112.90	1100	550.00	12	1163	12
**76Y	112.95	1100	550.00	36	1037	30
77X	113.00	1101	550.50	12	1164	12
**77Y	113.05	1101	550.50	36	1038	30
78X	113.10	1102	551.00	12	1165	12
**78Y	113.15	1102	551.00	36	1039	30
79X	113.20	1103	551.50	12	1166	12
**79	113.25	1103	551.50	36	1040	30
80X	113.30	1104	552.00	12	1167	12
80Y	113.35	1104	552.00	36	1041	30

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
81X	113.40	1105	552.50	12	1168	12
81Y	113.45	1105	552.50	36	1042	30
82X	113.50	1106	553.00	12	1169	12
82Y	113.55	1106	553.00	36	1043	30
83X	113.60	1107	553.50	12	1170	12
83Y	113.65	1107	553.50	36	1044	30
84X	113.70	1108	554.00	12	1171	12
84Y	113.75	1108	554.00	36	1045	30
85X	113.80	1109	554.50	12	1172	12
85Y	113.85	1109	554.50	36	1046	30
86X	113.90	1110	555.00	12	1173	12
86Y	113.95	1110	555.00	36	1047	30
87X	114.00	1111	555.50	12	1174	12
87Y	114.05	1111	555.50	36	1048	30
88X	114.10	1112	556.00	12	1175	12
88Y	114.15	1112	556.00	36	1049	30
89X	114.20	1113	556.50	12	1176	12
89Y	114.25	1113	556.50	36	1050	30
90X	114.30	1114	557.00	12	1177	12
90Y	114.35	1114	557.00	36	1051	30
91X	114.40	1115	557.50	12	1178	12
91Y	114.45	1115	557.50	36	1052	30
92X	114.50	1116	558.00	12	1179	12
92Y	114.55	1116	558.00	36	1053	30
93X	114.60	1117	558.50	12	1180	12
93Y	114.65	1117	558.50	36	1054	30
94X	114.70	1118	559.00	12	1181	12
94Y	114.75	1118	559.00	36	1055	30
95X	114.80	1119	559.50	12	1182	12
95Y	114.85	1119	559.50	36	1056	30
96X	114.90	1120	560.00	12	1183	12
96Y	114.95	1120	560.00	36	1057	30
97X	115.00	1121	560.50	12	1184	12
97Y	115.05	1121	560.50	36	1058	30
98X	115.10	1122	561.00	12	1185	12
98Y	115.15	1122	561.00	36	1059	30

TABLE 4.1. Continued

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
99X	115.20	1123	561.50	12	1186	12
99Y	115.25	1123	561.50	36	1060	30
100X	115.30	1124	562.00	12	1187	12
100Y	115.35	1124	562.00	36	1061	30
101X	115.40	1125	562.50	12	1188	12
101Y	115.45	1125	562.50	36	1062	30
102X	115.50	1126	563.00	12	1189	12
102Y	115.55	1126	563.00	36	1063	30
103X	115.60	1127	563.50	12	1190	12
103Y	115.65	1127	563.50	36	1064	30
104X	115.70	1128	564.00	12	1191	12
104Y	115.75	1128	564.00	36	1065	30
105X	115.80	1129	564.50	12	1192	12
105Y	115.85	1129	564.50	36	1066	30
106X	115.90	1130	565.00	12	1193	12
106Y	115.95	1130	565.00	36	1067	30
107X	116.00	1131	565.50	12	1194	12
107Y	116.05	1131	565.50	36	1068	30
108X	116.10	1132	566.00	12	1195	12
108Y	116.15	1132	566.00	36	1069	30
109X	116.20	1133	566.50	12	1196	12
109Y	116.25	1133	566.50	36	1070	30
110X	116.30	1134	567.00	12	1197	12
110Y	116.35	1134	567.00	36	1071	30
111X	116.40	1135	567.50	12	1198	12
111Y	116.45	1135	567.50	36	1072	30
112X	116.50	1136	568.00	12	1199	12
112Y	116.55	1136	568.00	36	1073	30
113X	116.60	1137	568.50	12	1200	12
113Y	116.65	1137	568.50	36	1074	30
114X	116.70	1138	569.00	12	1201	12
114Y	116.75	1138	569.00	36	1075	30
115X	116.80	1139	569.50	12	1202	12
115Y	116.85	1139	569.50	36	1076	30
116X	116.90	1140	570.00	12	1203	12
116Y	116.95	1140	570.00	36	1077	30

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
117X	117.00	1141	570.50	12	1204	12
117Y	117.05	1141	570.50	36	1078	30
118X	117.10	1142	571.00	12	1205	12
118Y	117.15	1142	571.00	36	1079	30
119X	117.20	1143	571.50	12	1206	12
119Y	117.25	1143	571.50	36	1080	30
120X	117.30	1144	572.00	12	1207	12
120Y	117.35	1144	572.00	36	1081	30
121X	117.40	1145	572.50	12	1208	12
121Y	117.45	1145	572.50	36	1082	30
122X	117.50	1146	573.00	12	1209	12
122Y	117.55	1146	573.00	36	1083	30
123X	117.60	1147	573.50	12	1210	12
123Y	117.65	1147	573.50	36	1084	30
124X	117.70	1148	574.00	12	1211	12
**124Y	117.75	1148	574.00	36	1085	30
125X	117.80	1149	574.50	12	1212	12
**125Y	117.85	1149	574.50	36	1086	30
126X	117.90	1150	575.00	12	1213	12
**126Y	117.95	1150	575.00	36	1087	30

TABLE 4.2. X/Y MODES FREQUENCY CORRELATION SUMMARY

VHF Channel Number	Frequency (MHz)	DME Operation Receive	DME Operation Transmit	LO Frequency 3 X Synth. freq.
108.0 TO 112.2 (0.1 MHz)	978 TO 1020	X		Above receiver frequency (receiver freq. +63)
108.0 TO 112.2	1041 TO 1083		X	
112.3 TO 117.9 (0.1 MHz)	1084 TO 1150		X	Below receiver frequency (receiver freq. -63)
112.3 TO 117.9	1157 TO 1213	X		
108.05 TO 112.35	1041 TO 1083		Y	Below receiver frequency (receiver freq. -63)
113.35 TO 117.55	1104 TO 1146	Y		
112.35 TO 117.95	1084 TO 1150		Y	Above receiver frequency (receiver freq. +63)
112.35 TO 117.95	1031 TO 1087	Y		

Dwg. No. TP00678

Spacing between pulse pairs

X = 12 microsec (0.1 MHz Channels)----------Both
Y = 36 microsec (0.05 MHz Channels)--Air to Ground
Y = 30 microsec (0.05 MHz Channels)--Ground to Air

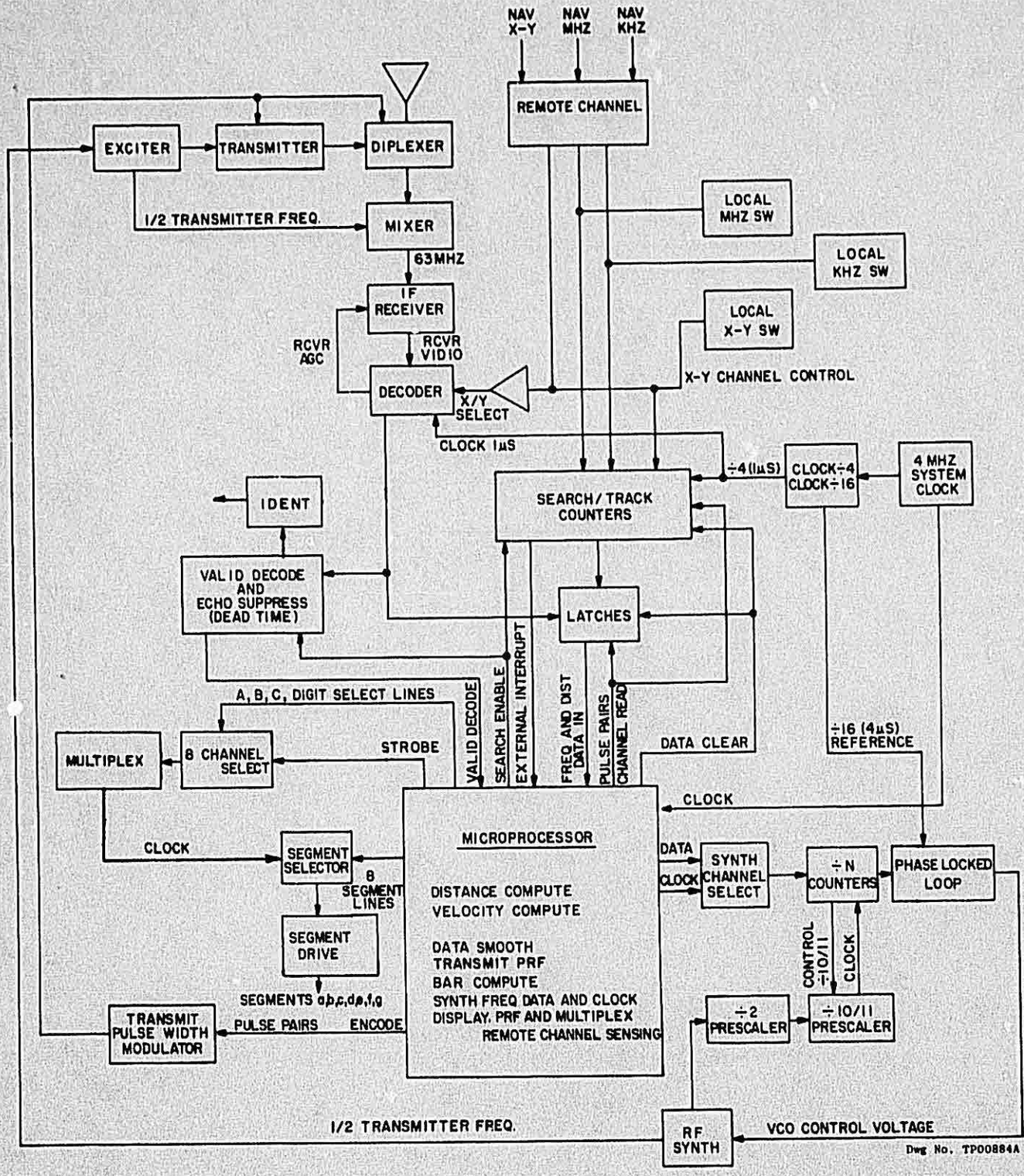


FIGURE 4-2. IDME 891 FUNCTIONAL BLOCK DIAGRAM

4.3 DME DISTANCE MODE OF OPERATION

The distance mode of operation will be described using Figure 4-2 as a guide.

The front panel 4 digit L.E.D. display normally indicates distance to station in nautical miles. The OBS Knob must be pushed in if velocity (KTS) information is required.

The transmitter is turned on as follows: The microprocessor generates pairs of pulses, 12 or 36 microseconds (us), at a PRF of 30 Hz. These pulse pairs are present at the "Encode" port of the microprocessor and act as reset pulses for the decoder and as trigger pulses for the transmit pulse width modulator. The pulse pair from the modulator turns on the transmitter. The Exciter stage of the transmitter runs continuously, whereas the first and final pulse stages and the Diplexer of the transmitter are turned on by the pair of 50V pulses from the Modulator. The Diplexer connects either the receiver or transmitter to a single antenna and protects the receiver from damage due to overload when the transmitter operates. The RF output from the antenna is pairs of pulses of RF energy at a selected frequency between 1041 and 1150 MHz. The pulses are 3.5 us wide having 12 us spacing on 0.1 MHz ("X" channels) and 36 us spacing on 0.05 MHz ("Y" channels). The synthesizer which operates at 1/2 the transmitter frequency, is injected into the Exciter section of the transmitter. The second buffer stage of the Exciter injects the 1/2 frequency into the Mixer where it is doubled and mixed with the incoming reply signal to give a 63 MHz IF that is now injected into the Receiver. Example: when the selected channel is 108.00, the transmit frequency is 1041 MHz, the synthesizer (Exciter) output is 520.5 MHz, and the receiver frequency 978 MHz. The received pulse pair (978 MHz) and Exciter frequency 520.5 MHz are combined in the mixer where the Exciter frequency is doubled (2 X 520.5 = 1041 MHz) and heterodyned with the received frequency of 978 MHz (1041 - 978 = 63 MHz). The pulse pairs are repeated at a 30 Hz rate. Approximately 50 us (equal to the ground station fixed delay) after the second pulse from the modulator turns on the transmitter, the microprocessor's search enable port enables the Dead Time Multivibrator, and turns on the search track counters. Now 1 us clock pulses feed three search track counters whose terminal count is 2048 us. The 1 us clock corresponds to the time required for the transmitted signal to travel 0.08 of a nautical mile and return. During the period that the Receiver is awaiting a reply from the ground station, the search track counters are measuring the time as they are being loaded with a train of clock pulses, one pulse for each 0.08 nautical miles to the ground station. With the modulation pulses removed from the Diplexer, the Receiver awaits the pulse pair reply from the ground station.

4.3 Continued

The 63 MHz IF frequency is amplified, detected, and converted to a logic level and fed to the Decoder. The Decoder confirms that the pulses of the received pulse pair are separated by the desired interval (12 or 30 us). The decoded reply is used as a clock pulse to transfer the accumulated count (present at the output of the Search Track Counters at the time of the received reply) into a latch. The microprocessor will accept this data only if the "Valid Decode" port goes logic low at the time of data from the latch transfer. The "Valid Decode" line is controlled by a Dead Time Multivibrator which is triggered by the decoded reply pulse. The Dead Time is approximately 60 us. Upon the initial trigger of this multivibrator, the microprocessor accepts the Search Track Counter Data, but during the 60 us Dead Time, any received decoded replies are ignored by the microprocessor. This Dead Time is used as an "Echo Suppression" (Signal Multipath), by holding off the decoder.

The microprocessor now compares this valid data with the valid data from a previous interrogation, if occurring at a synchronous rate, the microprocessor will do the following: compute the time between valid data which is equivalent to DME distance to ground station, and compute the rate of change of distance with time which is velocity. The displayed information of velocity is accurate only when flying directly to or from the station. When the Search Track Counters are started, they count through to the terminal count of 2048. The decoded reply does not stop the counters, only the instantaneous condition of the counters is sampled and stored. The microprocessor encodes the A,B,C select and segment lines used to illuminate the Display on the front panel. If there are no valid decoded replies for approximately 10 seconds the panel Display will signal a fault by displaying "bars" in place of the numerical distance display. This signifies to the pilot there is no accurate or useful information received by the DME.

4.4 DME OPERATION IN THE VELOCITY MODE

In the velocity mode, the DME continues to operate as in the distance mode, however, only velocity information is displayed. When the OBS Knob is pushed in to display velocity the display circuitry processes the proper A0A1A2 select and segment lines to present only velocity information.

4.5 REMOTE CHANNEL OPERATION

The IDME-891 is channeled by a companion NAV received (usually a MKI2D or NAV 824/825) whose remote channeling lines conform to the ARINC (2/5) code. This is the only way in which the DME can be channeled.

4.6 AREA NAVIGATION MODE (RNAV)

The IDME 891 has area navigation (RNAV) capability, but only with the RNAV 860 or NS 801 There are four input/output lines from the DME consisting of: RNAV Mode Control, RNAV data out, RNAV data in, and RNAV clock out. When the RNAV Mode Control line goes to logic low, the following events will occur: The microprocessor will send a serial clock and serial data (distance to VORTAC) to the RNAV, and accept serial input data (computed distance to the waypoint) from the RNAV. The distance displayed will be nautical miles to the RNAV WAYPOINT.

4.7 GENERAL

This circuit description supports the search track counters and the associated components necessary to present the microprocessor with valid information so it can compute the distance and velocity. Subsequent subsections separate these components and describe their operation in detail.

4.7.1 Microprocessor Cycle of Operation

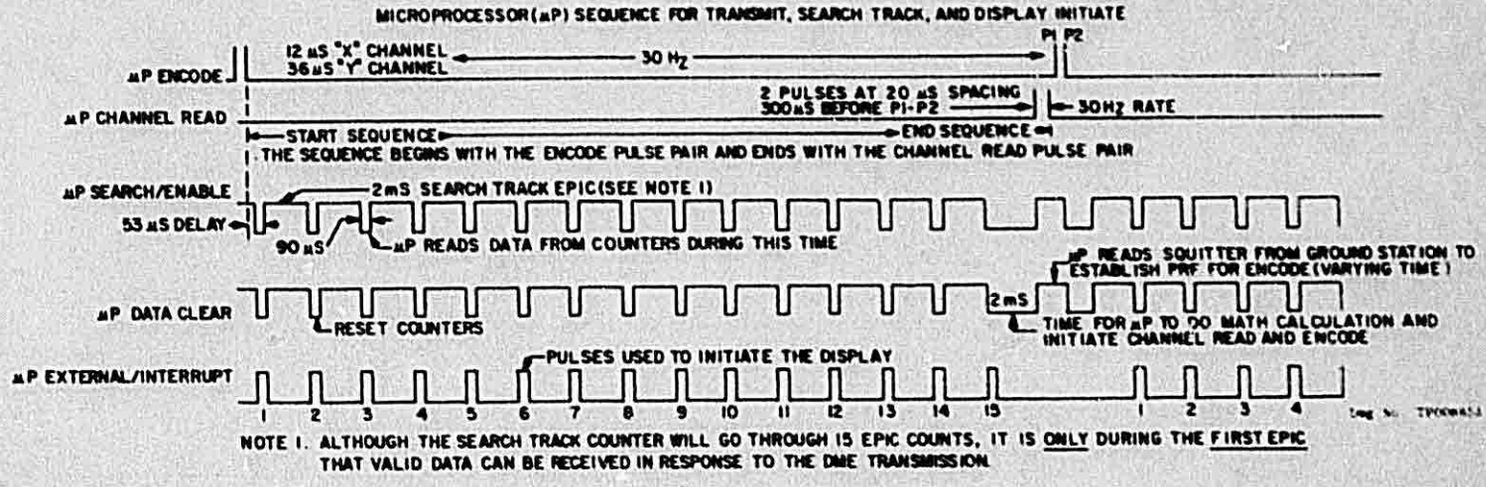
To facilitate the understanding of a Search Track Epic*, a routine the microprocessor follows will be described. Figure 4.3 is used as a guide.

1. The cycle begins with the microprocessor "Encode" port sending 12 or 36 us pulse pairs to the transmit modulator to turn on the transmitter.
2. 53 us later (this time is measured from the leading edge of the second encode pulse to the leading edge of the search enable pulse) the "Search Enable" line enables the Search Track counters for the terminal count (0-160 miles) of 2048 us. During the microprocessor's cycle of operation there will be a total of 15 terminal counts, however, it is only during the first terminal count, known as the "Search Track Epic", that valid information can be received in response to the transmission that occured 53 us prior to the beginning of the search track epic. The search enable line also enables the Dead Time multivibrator.
3. Concurrent with the search enable line, the "data clear" line is encoded and releases the latches and Search Track counters from their reset state. This line is active logic high for the Terminal Count.
4. At the termination of the count (2048 us), a pulse, EXT. INT. (external interrupt), is sent to the microprocessor. This pulse is used by the microprocessor in two ways:
   a. To signal the microprocessor to encode the segment lines for the display.
   b. As a clock to limit the number of external interrupt pulses to 15, at which time the microprocessor will take time out to do math calculations, read the ground station squitter which will be used to establish the transmitter PRF, and set up the Channel Read pulse pairs and the Encode pulse pairs.

* A Search Track Epic is defined as a transmission from the DME to the ground station, the reception and decoding of the ground stations reply transmission, an on-the-fly sampling of the Search Track counters elapsed time between transmission and reply, and the end of the 0-160 mile count (Terminal).

4.7.1 Continued

5. The cycle ends with the microprocessor generating a pair of "Channel Read" pulses which are used to sample the frequency control lines.



NOTE 1. ALTHOUGH THE SEARCH TRACK COUNTER WILL GO THROUGH 15 EPIC COUNTS, IT IS ONLY DURING THE FIRST EPIC THAT VALID DATA CAN BE RECEIVED IN RESPONSE TO THE DME TRANSMISSION.

FIGURE 4-3. MICROPROCESSOR ROUTINE

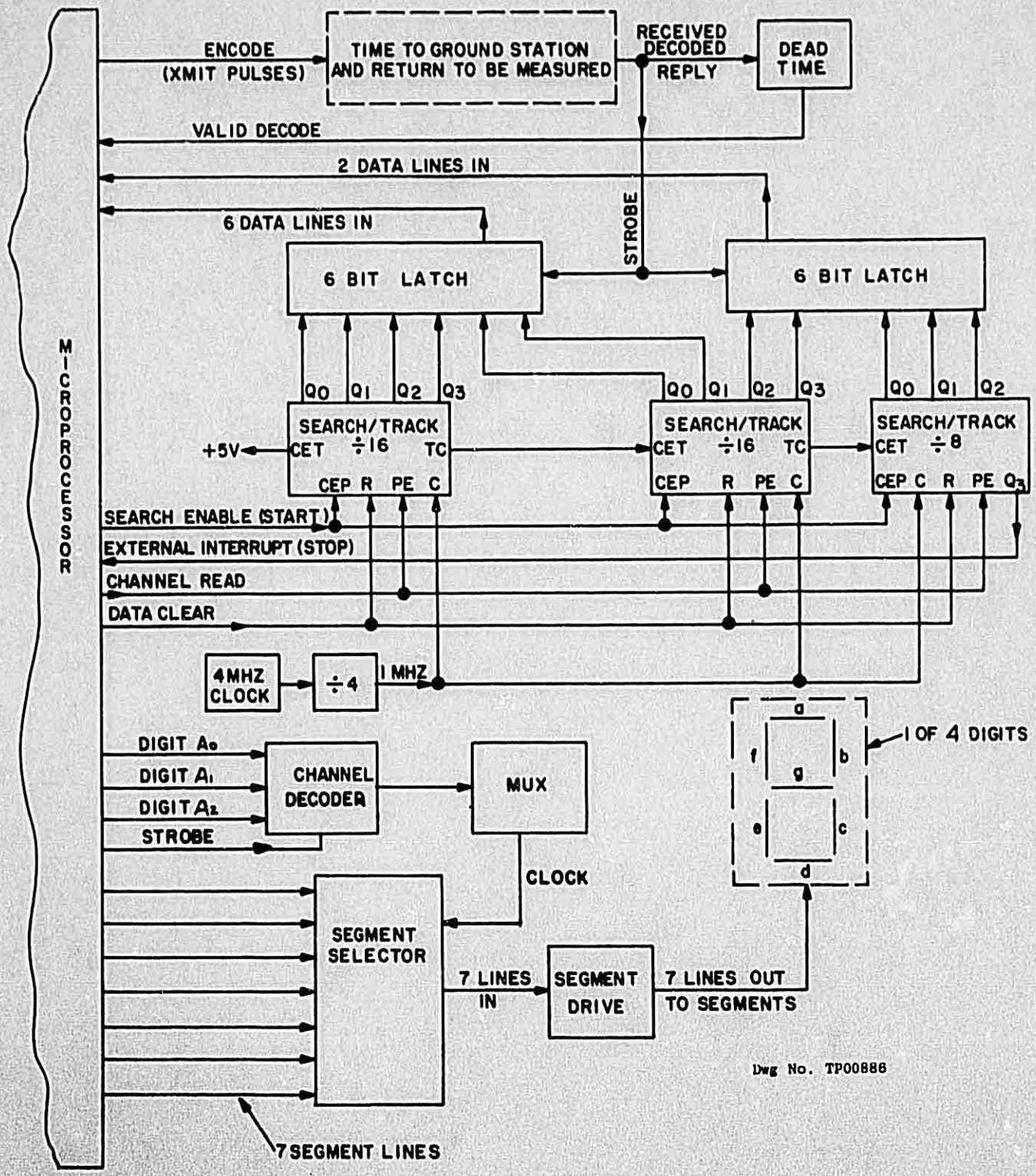


FIGURE 4-4. SEARCH TRACK EPIC

4.7.2 Search Track Epic

The front panel L.E.D display includes 4 digits and the extreme left digit never increases beyond "1". The displayed distance or velocity is the result of the valid data acquired from the ÷2048 search track counters during the search track epic. The capability of the display is considered to be 160 nautical miles. For the purpose of an explanation, one complete Search Track Epic will be described showing the method of data acquisition, the starting and stopping of the counters, and the display of the digits. (Refer to Figures 4-4, 4-5)

During actual operation, the display is in increments of 0.1 nautical mile. The Search Track Counters count increments of 1.0 microseconds obtained from the divided down (÷4) crystal controlled 4 MHz clock. The counters are started by the "Search Enable" port from the microprocessor 53 us after the "encode" port has turned on the transmitter. The 1 MHz clock pulses are fed into the counters without interruption. A single Search Track counter consists of four edge triggered "D" flip-flops (F-F) in series, capable of 16 counts. The counters output is in a binary format. Each of the four output lines is capable of indicating the logic state of its associated F-F, a "1" (high) or "0" (low). Also there is a Terminal Count (TC) output line which is fully decoded and is high only on the 15th count and returns to logic low on the 16th count. The TC output from the first counter is connected to the "Count Enable Trickel" (CET) input of the second counter, and the TC output of the second counter is connected to the CET input of the third counter. The Count Enable Trickle input must be logic high to enable the counter. A logic low at the CET input inhibits the count sequence and freezes the output lines in their existing states at the time the CET input goes logic low. The condition of each output line is shown in Figure 4-5.

To satisfy these operating conditions, apply the control signals to the Search Track Counters. The "data clear" line from the microprocessor has set all the counters and latches to their zero state (all four output lines are logic low). The uninterrupted 1 MHz clock is present at the clock input of the counters. The "search enable" line from the microprocessor goes to logic high, enabling the counters. As the clock pulses are loaded into the counter, the count progresses in a binary sequence as shown in Figure 4-5 and Table 4.3.

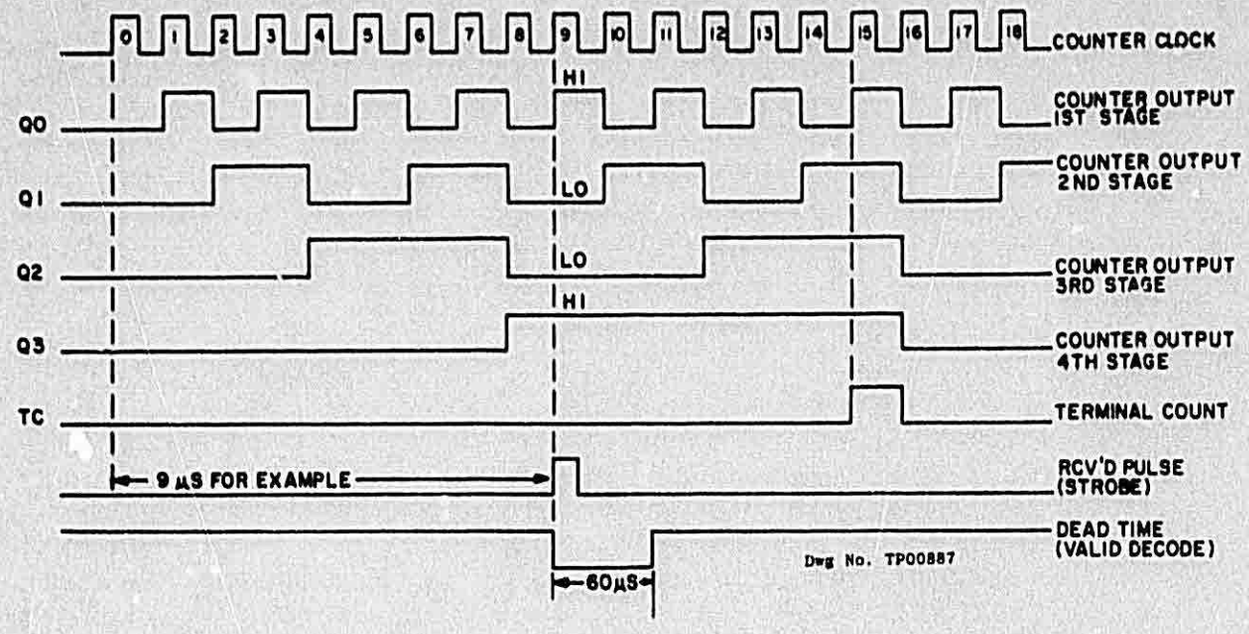


FIGURE 4-5. SEARCH TRACK TIMING DIAGRAM

TABLE 4.3. 4 BIT BINARY COUNTER

COUNT	OUTPUT			
	Qo	Q1	Q2	Q3
Reset 0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H
16	L	L	L	L

L= Low H=High

Dwg. No. TP00879

4.7.2 Continued

If, at the count of 9, a reply strobe pulse is fed into the 6 bit latches, as shown in Figure 4-5, the data at the latch inputs (Q0/Q3 are high, Q1/Q2 are low) will be transferred to the latch outputs for the microprocessor to read. At the same time the latches are being strobed, the "Dead Time" multivibrator is triggered (60 us), and its output is the "Valid Decode" input to the microprocessor. Upon receipt of the Valid Decode, the microprocessor accepts the data from the latches and during the 60 microsecond duration of the multivibrator it will not accept any new data. This 60 us Dead Time is to suppress echoes (signal multipath).

The counter continues the count sequence and upon reaching the 15th count the Terminal Count (TC) line goes logic high and enables the next counter. On the 16th count, the Q0 output of the 2nd counter changes state, and the TC line of the first counter goes logic low and freezes the 2nd counter while the 1st counter again starts its count sequence. Thus it can be seen that the 2nd counter is being enabled on by only 1-out-of-16 pulses so that in order to reach its terminal count of 16, there must be a total of 256 pulses (16 X 16). The 3rd counter needs 2048 pulses (256 X 8) in order for its Q3 output line to go high on its count of 8. This Q3 output from the 3rd counter is fed to the "External Interrupt" (EXT. INT.) port of the microprocessor and is used by the microprocessor in two principle ways:

1. As a command to light the display.
2. As a clock to limit the number of external interrupt pulses to 15.

At the conclusion of the Epic, the "data clear" and "search enable" lines go logic low to clear the counters and shut them down. After a period of approximately 90 us, the two lines go logic high to start another count. The microprocessor will initiate fifteen more terminal counts and at the conclusion of the 16th terminal count (see Figure 4-3) will shut down the Search Track counters for approximately 1 ms. During this off period, the microprocessor is doing math calculations and setting up the sequence of reading ground station squitter, initiating channel read and encode pulse pairs. At the conclusion of the 1 ms shutdown, the microprocessor starts the Search Track Counters and samples the ground station squitter which it will use to establish the "Encode" PRF rate. Next, the microprocessor shuts down and clears the Search Track Counters and then issues a "channel read" command consisting of 2 pulses. The first pulse will load the frequency control lines data into the Search Track Counters and upon receipt of the next Search Track Counter 1 MHz clock pulse, transfers this data to the inputs of the 6 bit latches. The 2nd "channel read" pulse strobes the 6 bit latches and transfers this data into the microprocessor where it is compared to the previous "Channel Read" data.

4.7.2 Continued

When the microprocessor compares the current data with the previous data and they agree, no change will occur in the display. However, if the data does not agree because the pilot has selected a new frequency, then the microprocessor will initiate the following action:

1. Encode the synthesizer channel data and clock lines to update the synthesizer frequency. This occurs only once.
2. Cause "bars" to appear in the distance section of the display.
3. When the DME locks on to the new station approximately 4 seconds later, the display will automatically read Distance.

Upon receipt of each EXT. INT. pulse at the end of each terminal count the microprocessor will send a "strobe" pulse to enable the display decoder and encode the A0A1A2 select and segment lines to light the display.

4.8 DETAILED CIRCUIT DESCRIPTION

4.8.1 Transmitter Modulator

Refer to the Range Board Schematic (Section 6) for the following discussion.

The Modulator turns on the transmitter when directed to by the Encode port of the microprocessor. The Modulator is separated into a pulse width control section and a driver section. The Encode port triggers the pulse width multivibrator (U308A) at a PRF of 30 Hz with a pair of pulses whose spacings are 12 microseconds (us) (X channel), or 36 us (Y channel). The period of U308A is adjusted by R331 to set the width of the transmitter's output pulses to 3.5 us.

The modulator driver received +60 volts from the power supply and Zener diode CR305 regulates this at 51V. This 51V is the supply voltage for the transmitter and Modulator drive transistor, Q301. In the quiescent state, the base of Q301 is clamped one diode junction above the 51V Zener voltage and is sitting at 51.7V. Clamp diode, CR304, prevents the base/emitter voltage of Q301 from exceeding its rated reverse breakdown of 5V. When U308A is triggered, its Q2 (pin 13) and $\overline{Q2}$ (pin 4) outputs turn on Q302. Q302 pulls the base voltage at Q301 down, thereby turning on Q301. Q301's collector rises to 50V for a period of 3.5 us for each trigger pulse. (These pulses are used to modulate Q206, the pedestal modulator, in the Exciter section of the transmitter and Q102, the final transmitter modulator).

4.8.2 Transmitter

The Transmitter amplifies the RF excitation from the Synthesizer and doubles it's frequency when pulsed by the Modulator. The transmitter comprises 4 basic functional areas as shown in Figure 4-6, CW amplifiers Q201, Q202, Q203, and Q204, first pulse amplifier Q205, frequency doubler Q101, and final amplifier Q102. When provided with an excitation level of +3 dBm at 550 MHz, the exciter output frequency range is from 520.5 through 575 MHz and the transmitter output from 1041 to 1150 MHz, however, to simplify this description, the input and output frequencies will be 550 and 1100 MHz respectively.

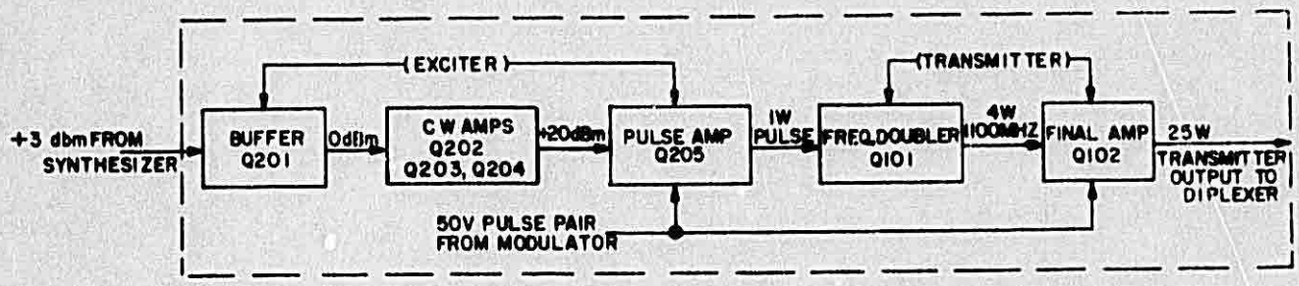


FIGURE 4-6. RF TRANSMITTER FUNCTIONAL BLOCK DIAGRAM

4.8.2.1 Exciter (low level RF amplifier) Refer to Transmitter Schematic.

The Exciter is a 5 transistor RF amplifier that provides 1 watt (+30 dBm) of pulsed drive to the frequency doubler, Q101. A resistive attenuator (R210, R211, R212) provides isolation between transmitter and synthesizer. C201 is the coupling capacitor to the input buffer stage, Q201. Q201's output is RC coupled to Q202, Q203, Q204, Q205, Q101, Q102. These capacitors, together with inductors L201, L202, L203, and L204, form the interstage matching networks. L205 and L101 are RF chokes.

Functionally, the Q203/Q204, and Q204/Q205 interstage coupling are identical. Each output stage uses a pair of capacitors as a divider network with one of the capacitors being adjustable so as to match the impedance between stages for maximum transfer of power. The output of Q202 is delivered to a special 50 ohm power splitter, T201, whose purpose is to split the signal into two paths, one going to the mixer at a 0 dBm level, and the other to Q203 at the same 0 dBm level. Q203 delivers a +10 dBm level to Q204 and Q204 delivers +20 dBm level to Q205. Part of the interstage coupling network between Q205 and the frequency doubler Q101 is a coaxial cable (Z201) cut to 1/4 wavelength which transforms the high impedance required at Q205's output, to a low impedance at Q101's input. This type of matching is necessary because the impedance looking into the emitter of Q101 is very low.

4.8.2.1 Continued

Separate decoupling circuits are used in Q202 and Q203 stages. C203 and C204 are used for RF bypass and R203 and R204 are used for decoupling from the +14 volt power supply.

All 5 stages of the Exciter receive base bias through voltage dividers (i.e. Q201 uses R201 and R213), and operate as Class A amplifiers. However, with no DC bias, Q101 and Q102 operate as Class C amplifiers. Upon receipt of a pair of 50 volt pulses from the pulse modulator, the pedestal modulator transistor, Q206, is turned on. These 50 volt pulses are Zener regulated down to 33 volts by CR201. The 550 MHz RF is continuously applied to Q205's input, when the 33 volt pulses are applied to the collector, the RF is gated on and this output is applied to the transmitter frequency doubler, Q101. The drive into Q101 is 1 watt of pulsed power.

4.8.2.2 Transmitter Doubler and Final Amplifier

The negative excursions of the pulsed RF applied to the emitter of Q101 turn this frequency doubler on. The 550 MHz is half-wave rectified, and according to theory, contains all the discrete numbered multiples (i.e. 1-2-3-4----) of the fundamental applied frequency, 550 MHz. At the collector of Q101 is a 1/4 wavelength, open coaxial cable (Z101) that acts as a RF short to the 550 MHz and as a high impedance to the 2nd harmonic, 1100 MHz. The power developed at the collector of Q101 is 4 watts and is coupled into the final amplifier, Q102. The impedance matching network coupling Q101 and Q102 consists of etched printed circuit transmission lines with adjustable capacitor, C101, providing the means for making an optimum match.

At the same time the pedestal modulator transistor (Q206) is turned on, the final amplifier modulator (Q104) is also turned on, however, the combination of R105 and L109 form a delay network to insure that the pulsed RF energy from Q101 will arrive at Q102 before Q102 is gated on. The reason for this is to insure that the final transmitted pulse pair will have the correct shape. The purpose of L110 at the emitter of Q104 is to provide a DC return path. The output from Q102 is 25 watts of pulse power. This is coupled through etched printed circuit transmission lines to the Diplexer.

4.8.3 Diplexer Receiver and AGC Circuits

Shown in Figure 4-7 are the receiver circuits in block form. RF energy is routed to the Band Pass Filter (BPF) by the Diplexer. BPS output energy is amplified by the RF amplifier and then mixed with the local oscillator signal from the power splitter T201, to produce a 63 MHz IF signal. This signal is then amplified in the receiver's 63 MHz IF amplifier, video detected, amplified and clipped to a 5 volt logic level and then sent to the Decoder.

The Decoder delays the video data for 12 microseconds (us) on X channels or 30 us on Y channels. Properly spaced pulse pairs will result in delayed data from the Decoder, and Video data to the Decoder, arriving coincidently at U309's AND gate inputs. A pulse from the AND gate will then enable the Sample and Hold AGC circuit that will then sample the Video amplifier's pulse amplitude and produce an AGC voltage for the 63 MHz IF circuits.

4.8.3.1 Diplexer and Band Pass Filter

The Diplexer alternately connects the antenna to the receiver or the transmitter as directed by the 33 volt pedestal modulator pulse pair. In the transmit mode, the positive going pedestal pulses will back bias PIN diode CR102, isolating the receiver. Diode CR101 connects the transmitter output, through C102, to the antenna.

This provides the necessary isolation between the transmitter and receiver. Inductor L103 is the DC return path for diode CR102 and L104 is the DC return path for diode CR101.

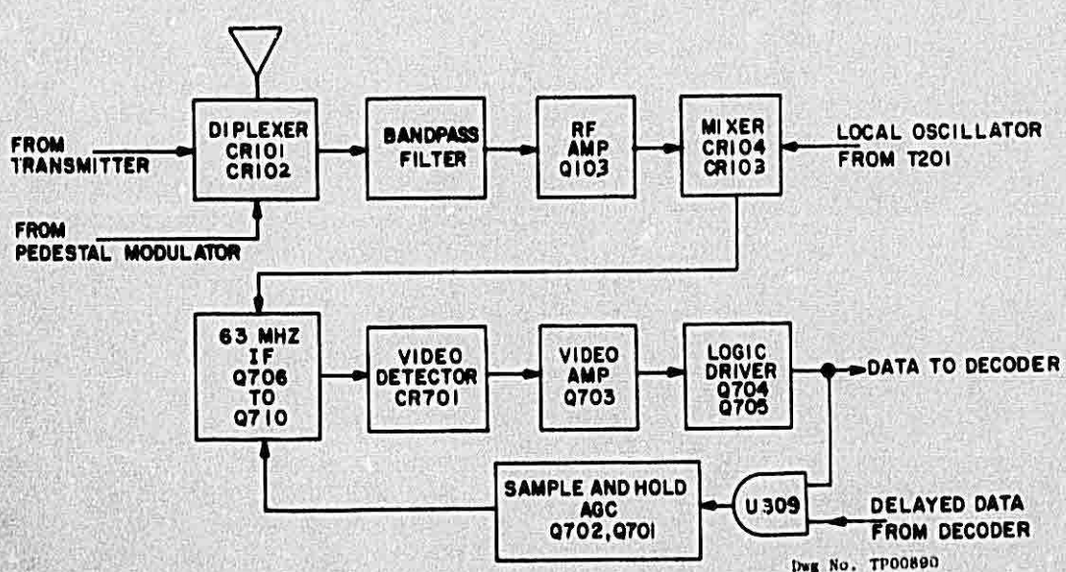


FIGURE 4-7. RECEIVER BLOCK DIAGRAM

4.8.3.2 RF Amplifier and Mixer

The RF amplifier consists of a low noise UHF transistor (Q103) stage which provides a gain of 8 dB over the frequency range of 978 to 1213 MHz. In addition to increasing the level of the incoming RF signal, it also acts as an isolation to the local oscillator signal in the mixer, preventing CW antenna radiation. L108 parallel resonates the parasitic capacity of Q103 and C105 couples the received signal into the mixer.

The local oscillator (LO) injection, which is 1/2 the frequency of the transmitter, is coupled into the mixer through the series resonant combination of C104 and L106. The harmonics generated in the mixer will be isolated from the Exciter as this series L and C is seen as a high impedance to these frequencies. Mixing occurs in diodes CR103 and CR104 where the LO and Receiver RF signals are heterodyned, the 2nd harmonic of the LO with the received frequency provides a difference frequency of 63 MHz. The inductor L105 is a low impedance to 63 MHz and passes this signal to the IF Amplifier, however, its impedance to higher frequencies effectively isolates them from the IF Amplifier.

4.8.3.3 IF Amplifier and Detector (Refer to Receiver Schematic)

The five stage IF amplifier, Q706 thru Q710, is comprised of a 63 MHz 6 pole filter consisting of 3 double-turned interstage networks and a single tuned coil, L701. AGC voltage is applied to each of the IF transistors with the gain being proportional to the amount of AGC voltage available to supply base current to each transistor. The +14 volt supply to each collector is RF bypassed by a 1000 pF capacitor and decoupled by a 100 ohm resistor.

The 63 MHz energy from the Mixer is amplified and filtered by Q708, Q709, Q710, and further amplified by the two stage amplifier, Q706 and Q707. The signal at the collector of Q706 is coupled into a series resonant combination consisting of C708 and L701. This combination is broadly resonant at 63 MHz and the amplitude of the signal across L701 is greater than that across C708. This RF signal must now be video detected which is the purpose of Schottky diode, CR701. In addition to resonating with C708, L701 is the DC return for CR701.

The signal to be detected consists of two 3.5 microsecond (us) Gaussian bursts of 63 MHz energy. The negative excursion of the signal turns on CR701 and charges C702. The RC time constant of R702 and C702 is slightly greater than 3.5 us and far greater than the time of one cycle of 63 MHz. Thus when CR701 is initially turned on, C702 receives a negative charge, then, during the positive excursion the RF signal back biases CR701. C702 does not have enough time to recover its positive charge and C702 remains negative until the signal ends and C702 regains its positive potential. Therefore, the detection process is the formation of a negative pulse at C705 whose width is equal to the 3.5 us burst.

The purpose of L702 is to block 63 MHz energy from the Video Amplifier.

4.8.3.4 Video Amplifier and Logic Driver (Refer to Receiver Schematic

Video amplifier, Q703 is normally biased on, thus operating Class A, while logic drivers Q704 and Q705 are biased off. The gain of Q703 is approximately 200 which increases the detected video pulse amplitude to about 1 volt peak-to-peak. The negative detected pulse at C705 reduces the base current in Q703 generating a positive pulse at its collector turning Q704 on. As Q704 turns on, its collector goes negative with respect to the emitter of PNP Q705 and turns on Q705 pulling the junction of R708 and R711 up to 7 volts.

This squared pair of 7 volt peak-to-peak pulses is of correct logic level to drive the decoder, U301. Diode CR702 clamps to ground any negative pulses, which would interfere with the AGC Sample and Hold circuitry.

4.8.3.5 Sample and Hold AGC (Refer to Receiver Schematic)

The Sample and Hold AGC controls the IF gain to produce uniform amplitude pulses at the output of the Video amplifier. In addition, only properly spaced pulses will enable AGC action. Proper pulse spacing is determined by AND gate U309. The receiver video pulses are applied to U301, the Decoder, and U309. The Decoder delays the receiver video pulses 12 us on X channels or 30 us on Y channels. Delayed data from the Decoder is applied to U309. If properly spaced, the second Video pulse from the receiver will occur coincident with the delayed first video pulse from the Decoder thereby generating a single pulse at the output of U309. This pulse will turn on Q702, and as a result, video pulses from the voltage divider R704 and R709 are gated from the collector of Q702 to the emitter and charge up holding capacitor C703. These sampled video pulses cause Q701 to conduct. Normally, transistors Q708 thru Q710 receive bias from the +14 volt supply which is divided down by R701 and each 470K base resistor (R714, R717, R720, R823, R726). When video pulses turn on Q701, the AGC voltage is reduced according to the amplitude of these pulses. Therefore, the gain of the IF stages is automatically controlled.

4.8.4 Decoder

4.8.4.1 General

The purpose of the Decoder is to examine the received signals for proper pulse spacing (i.e. either 12 or 30 us). Incorrectly spaced pulse pairs are rejected while correctly spaced pulse pairs are accepted and routed to the Receiver AGC circuitry, and Dead Time multivibrator.

4.8.4.2 Theory (Refer to Range Board Schmatic)

The Decoder is comprised of a shift register (delay line) U301, Coincident AND gate U309D, and X-Y channel select inverter U310A as shown in Figure 4-8. The shift register functions as a digital delay line operating in a serial-in/serial-out mode with clock pulses shifting the data at a 1 microsecond rate. The length (delay) may be programmed to any number of bits between 1 and 64 by applying the proper logic 1 (high) or logic 0 (low) to the control inputs (L1, L2, L4, L8, L16, L32). (See Table 4.4)

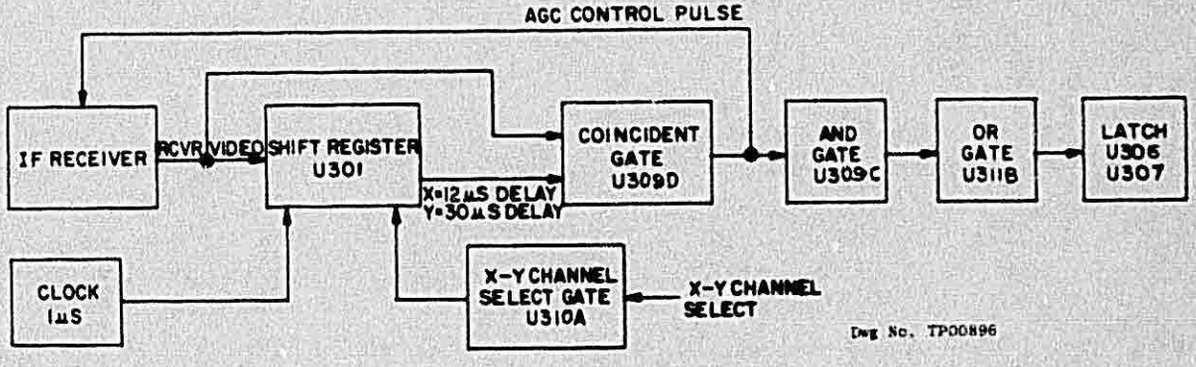


FIGURE 4-8. DECODER BLOCK DIAGRAM

TABLE 4.4. U301 PROGRAM

CONTROL IMPUTS						REGISTER LENGTH	CHANNEL
L32	L16	L8	L4	L2	L1	MICROSECONDS	
0	0	1	1	0	0	12	X
0	1	1	1	1	0	30	Y

Dwg. No. TP00880

4.8.4.2 Continued

Table 4.4 shows the programming for the X-Y channels.

When the shift register is programmed for an X channel the register is clocked at a 1 us rate and 12 clock pulses thus provides a delay of 12 us. Y channel is represented by 30 clock pulses equaling a 30 us delay.

At the beginning of a Search Track Epic, the Encode port (pin 3) of the microprocessor sends 2 pulses to the reset (R) input of U301 and Q output (pin 10) will be set to logic 0. When a reply is received, the first receiver Video pulse (P1) is differentiated by C310 and R319 and applied to U301, pin 6. Diode CR302 clamps the negative differentiated spike to ground which protects the CMOS U301. The 1 us clock pulses begin to shift (delay) the data (P1). After 12 us, P1 appears at the Q output of U301 and is applied to pin 2 of U309D (Coincident AND Gate). At the same time, the second receiver Video pulse (P2) appears and is applied to pin 1 of U309D. Since both P1 and P2 are present at the same time, a single pulse appears at the output of U309D, pin 3. Thus, only properly spaced replies can pass through U309D.

The decoder reply from U309D is used in three ways:

(1) It is used by the IF Receiver to enable the AGC Sample-and-Hold (AGC control pulse).
(2) It is used as a trigger for U308B the Dead Time Multivibrator.
(3) It is used as a strobe for the latches, U306 and U307.

When U308B (Dead Time) is triggered, U301 will be shut down for approximately 60 us as the Q, output from U308B, pin 5 is applied to the reset (R) of U301.

4.8.4.3 Dead Time Multivibrator (Refer to the Range Board Schematic)

The Dead Time Multivibrator, U308B, serves to reduce the possibility of synchronizing the DME to a reflection path (Echoes). The chances of this happening at shorter ranges is much greater than at longer ranges, hence, the Dead Time of 60 us corresponds to a range of approximately 5 nautical miles.

U308B is a retriggerable, resettable multivibrator. Table 4.5 shows the A-B excitation and the response to those inputs.

At the start of a Search-Track Epic, the Search Enable line is logic low and prevents U308B from being triggered. 53 us later the Search Enable line goes logic high for the duration of the 0-160 mile count, and is inverted by U310B. U308B is now primed and ready to be triggered. Upon receipt of a valid decoded pulse (trigger) from AND gate U309C, U308B is triggered for a dead time of 60 us. The Q output is OR'ed by U311A and shuts down the Decoder, U301. The $\overline{Q}$ output of U308B is the Valid Decode input signaling the microprocessor to accept the data from the latches.

TABLE 4.5. U308B EXCITATION

INPUTS		
A	B	RESPONSE
⌐	L	NO TRIGGER
⌐	H	TRIGGER
H	⌐	NO TRIGGER
L	⌐	TRIGGER

⌐ ← This symbol means an input transition from Logic High to Logic Low.

⌐ ← This symbol means an input transition from Logic Low to Logic High.

H=Logic High, L=Logic Low
Dwg No. TP00882A

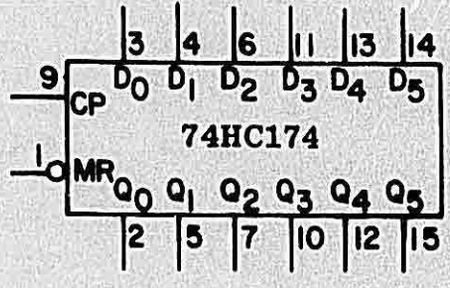
4.8.5 Search Track Counters and Latches

The microprocessor commands the Search Track Counters and Latches to operate in either of three modes: Search Track, Channel Read, and display interrupt. The microprocessor has a routine that it has been programmed to follow. Briefly that sequence is as follows: the microprocessor will initiate 15, 0-160 mile counts (a 0-160 mile count is the time taken by the counter chain to reach its terminal (end) count), and then briefly interrupt this sequence to perform various calculations, and then issue a Channel Read command.

4.8.5.1 Search Track Sequence Mode

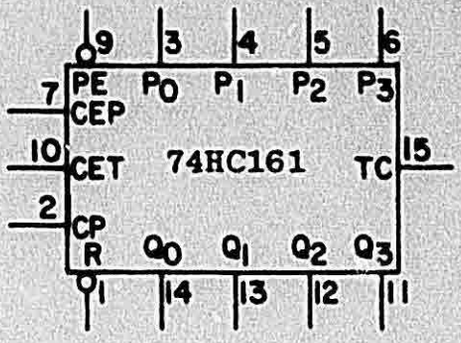
The purpose of the Search Track Mode of operation is to measure the elapsed time between the DME transmission and the ground station reply. This is accomplished by counting 1 microsecond intervals (equivalent to 0.08 mn) between airborne transmission and ground reply with a delay that cancels the Ground Stations delay.

Before proceeding with the circuit theory, a functional description of a 74HC174 latch and 74HC161 counter will be given so that their operation may be fully understood.



The 74HC174 is a high speed Hex D Flip-Flop. The information on D inputs (D0 to D5) is transferred to storage (Q0 to Q5) during the LOW to HIGH clock transition (CP). The device has a Master Reset (MR). A logic LOW to the MR input will force all Q outputs to logic LOW, independent of clock or data inputs.

4.8.5.1 Continued



The 74HC161 is a 4 bit synchronous binary counter that counts up to 16 in a binary sequence. It features a synchronous Parallel Enable (load). All changes of the Q outputs occur as a result of, and synchronous with, the LOW to HIGH transition of a Clock input (CP).

Three control inputs, Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) select the mode of operation. The Count Mode is enabled when the CEP, CET and PE inputs are logic HIGH. When the PE is logic LOW, the counters will synchronously LOAD the data from the parallel inputs (P0, P1, P2, P3) into the counter on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit (HOLD) the count sequence. With the PE held logic HIGH, a logic LOW on either the CEP or CET inputs will cause the existing output states (Q0, Q1, Q2, Q3) to be retained.

The Terminal Count (TC) output is logic HIGH when the CET input is HIGH and the counter is in the 15th count of its sequence. On the 16th count, theTC returns to LOW.

The Reset (R) input, when logic LOW, overrides all other input conditions and sets the Q outputs to logic LOW.

4.8.5.1 Continued

53 microseconds after the Encode port of the microprocessor has initiated a DME transmission, the Search Enable port goes logic HIGH and enables the Search Track chain. Concurrent with the Search Enable line, the data clear line goes logic HIGH releasing the counters and latches from their reset state. The Channel Read line, which is normally LOW is inverted by U310E and sets the counters to the Count Mode.

U302 feeds 1 us clock pulses continuously to the counters (U303, U304, U305) which run uninterrupted to the final count of 2048.

TABLE 4.6. BINARY CODE

OUTPUTS					CLOCK PULSE NUMBER
TC	Q3	Q2	Q1	Q0	
0	0	0	0	0	Start
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
1	1	1	1	1	15
0	0	0	0	0	16

Dwg. No. TP00881

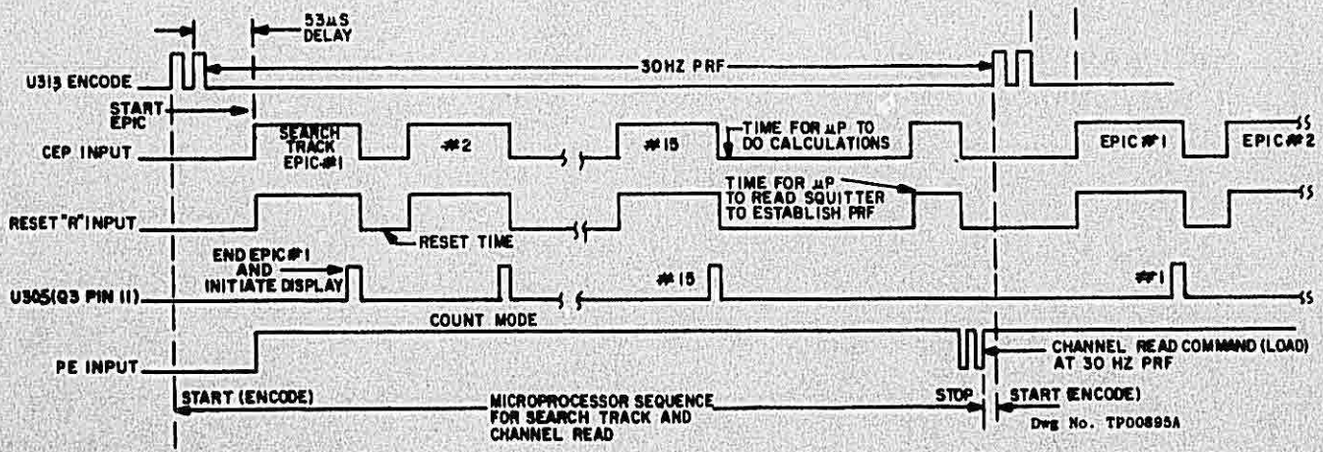


FIGURE 4-9. U303, U304, U305 CONTROL INPUTS

4.8.5.1 Continued

U304 and U305 are initially inhibited since their CET inputs are connected to the TC output of the preceding counter and are in a logic LOW state. (Refer to Range Board Schematic) U303 begins counting and at the 15th clock pulse its TC output goes logic HIGH. This releases U304 from its HOLD state and upon receipt of the 16th clock pulse, Q0 of U304 goes to logic HIGH, and the TC output of U303 goes back to logic LOW and puts U304 back in the HOLD state. U303 again goes through its count sequence which results in the Q1 output of U304 changing to logic HIGH. It has taken 32 clock pulses for U304 to reach the count of 2. In order for U304 to reach the count of 15 and release U305 from its HOLD state, it will take 255 clock pulses. During one 0-160 mile count, there will be 128 TC output pulses from U303 and 8 TC output pulses from U304. The Q3 output from U305 is connected to the External Interrupt (EXT INT) port, pin 38, of U313. A logic HIGH signals the microprocessor to end the 0-160 mile count, start another and initiate the display. Since Q3 of U305 will go logic HIGH on its count of 8, it will take a total of 2048 (256 X 8) clock pulses to end the count. The microprocessor will use the EXT INT pulse as a display initiate and as a clock to limit the number of 0-160 mile counts to 15, at which time it briefly enters into a different routine. The Data Clear (counters reset) time between each of the 15 counts is approximately 90 us.

A reply pulse pair that is received during a Search Track epic and is recognized by the decoder, will strobe latches, U306 and U307, and U308B the Dead Time Multivibrator. The outputs from the counters, at the time of the latch strobe from U311B, will be transferred to the latch outputs for the microprocessor to read. The latch strobe does not stop the counters, it only samples their outputs.

During a later routine in its program, the microprocessor will review all this stored data in its memory banks and make comparisons to sort out the valid synchronous replies from the noise and ground station squitter. This data will be smoothed and used by the microprocessor to compute distance and velocity information. If for any reason, valid replys are not received for 10 seconds or longer, the microprocessor will signal a fault by causing "bars" to be displayed in place of the distance readout.

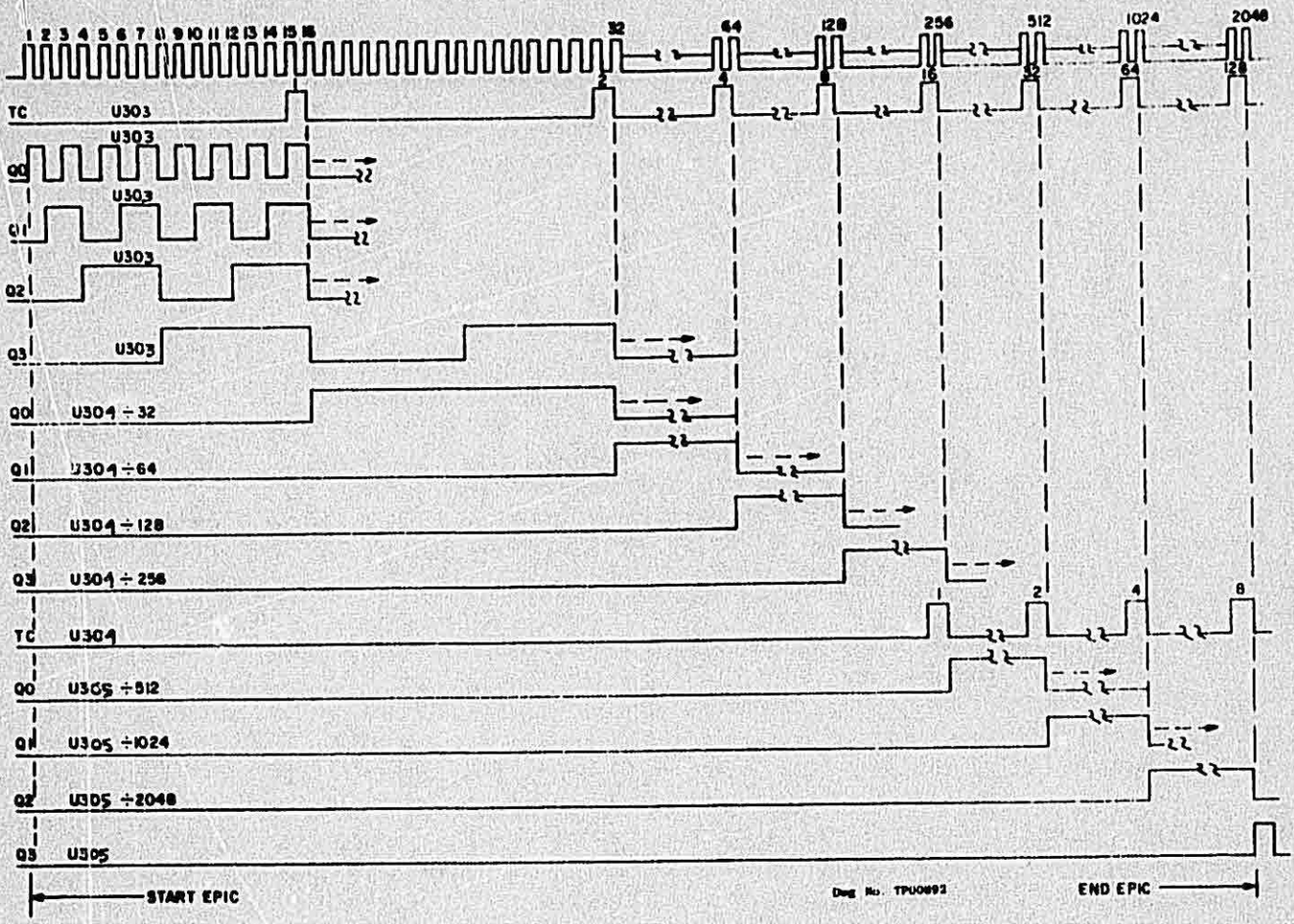


FIGURE 4-10. SEARCH TRACK COUNTERS TIMING FOR 1 EPIC

4.8.5.2 Channel Read Sequence Mode (Refer to Range Board Schematic)

The purpose of the Channel Read Sequence is to sample the frequency control lines at a 30 Hz rate and latch this information for the microprocessor to read. At this point serial data can be sent to the digital control section of the synthesizer, in the event frequency has been changed.

In addition the following are also sampled at a (30 PRF): The RNV mode line, and X-Y channel line.

The last routine in the microprocessor's cycle is to issue a Channel Read command. This consists of a pair or positive pulses from the Channel Read port, pin 16, of U313 which initiates the following action:

a) The Channel Read pulses are inverted by U310E and fed to the Parallel Enable (PE) inputs of the Search Track Counters. A logic LOW into the PE sets the counters into a LOAD condition and upon the receipt of the next 1 us clock pulse, the data present at the parallel inputs (P0-P3) is transferred to the outputs (Q0-Q3).

b) The channel read pulses are OR'ed by U311B and strobes the latches U306, U307, which transfers the data present at D0 to D5 to the latch outputs where it is read by the microprocessor.

When a frequency is first selected, the microprocessor will issue only <u>one</u> set of data to the synthesizer digital logic control. Thereafter, as it samples the frequency control lines, it will compare new data to the old, and if the same, will take no action. However, when a new frequency is selected, the new data will not compare with the old so the microprocessor will again issue only one set of new data to the synthesizer logic.

The IDME 891 uses 4 lines of the ARINC 2/5 code for frequency selection. The DME's frequencies are selected at a remote (separate) NAV receiver.

4.8.5.2.1 Remote Channeling

The IDME 891 does not have channeling switches. It can only be remotely channeled by its companion NAV receiver that uses the ARINC 2/5 code.

The remote channeling circuitry consists of isolation resistors (100 K) R301 to R309 and pull up resistors (680K) R310 to R318.

When there are no connections to the remote channeling lines or the lines are open circuited by the NAV receivers, the lines will all be pulled up to 5 volts. The microprocessor will sense this unique condition and signal a fault by causing the L.E.D. display to show "bars".

If the OBS knob is pushed in (velocity mode) the display will show the letters "Err" (error).

The X-Y channel line is connected to counter U305 and also to decoder U301 via inverter U310A which programs the decoder for an X channel delay of 12 us or a Y channel delay of 30 us. Counters U303 and U304 are used to extract the ARINC channeling data for the microprocessor to read. If the DME is channeled to a new frequency, for a period of 4 seconds after the channeling change, the new frequency can be read in the IDME's L.E.D. display if the OBS knob is pushed in to select the velocity mode of presentation.

The X-Y line input to counter U305 is used to signal the microprocessor to encode an X channel pulse pair of 12 us or a Y channel pulse pair of 36 us spacing.

4.8.6 Ident Audio

The Ident Audio is extracted from the dead time multi U308B. U308B is toggled by the signal obtained from the decoder AND gate, U309D and U309C. This can be noise, squitter, or Ident signal. The Ident signal is a Morse code identification of the ground station at 1350 Hz, actually, a regular PRF of 2700 Hz (1350 double pulses). When not transmitting Ident, the ground station transmits squitter, a random output of approximately 2700 pulse pairs per sec.

The trigger input from U309C is a positive decoded pulse comprising 2700 squitter pulses per second. Since these pulses are random, the Ident output sound is similar to that of noise. However, when Ident is being transmitted, the sound of the 1350 pulse pairs per second tone resembles the output of a tone generator.

These 5 volt level 1350 pulse pairs are coupled thru C338 and parallel connected to 4.7K (R341) and 47K (R342) resistors creating two audio levels that are available at rear connector P301 pins 10 (low level) and 29 (high level).

4.8.7 Clock Generator

The clock generator provides timing pulses to the microprocessor, decoder, search track counters and the phase locked loop of the synthesizer. The clock generator comprises a crystal controlled 4.000 MHz oscillator driving the microprocessor and a 4 bit ripple counter as shown in the Range Board Schmatic.

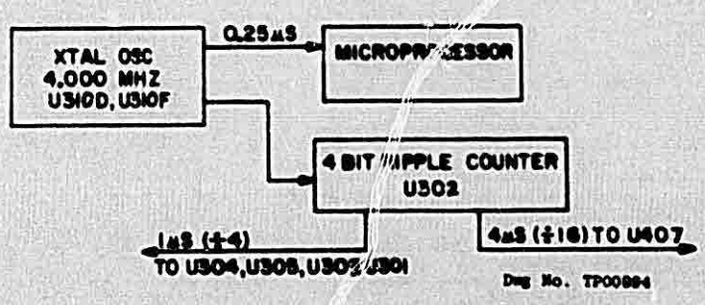
In the following description, the pulse periods are given on the basis of the interval between the leading edge of adjacent pulses.

The period is much easier to read and check from the calibrated time base of an oscilloscope.

The crystal oscillator comprises two inverters within U310. The first section, U310F utilizes R325 to set the operating range in its linear region. The second stage, U310D, serves as an inverter, whose output, through capacitor C319 and crystal Y301 provides the positive feedback necessary to sustain oscillation at the crystal frequency. The clock drives the microprocessor and counter U302.

U302 is a 74HC93 4 bit ripple counter. The master resets (pins 2 and 3) are grounded permanently, enabling the counter. The 4 MHz clock pulses are applied to input CPO. Simultaneous divisions of 2, 4, 8 and 16 are performed at Q0, Q1, Q2 and Q3 outputs when the output of Q0 is externally connected to input CP1.

The divide by 4 output (Q1) provides 1 us clock pulses to the decoder U301, and Search Track counters U303, U304, and U305. The 1 us period is equivalent to 0.08 nautical mile. The divide by 16 output (Q3) provides a 4 us (250 KHz) reference clock to the phase locked loop, U407.



4.8.8 Frequency Synthesizer Description

Refer to the VCO/Synthesizer Schematic.

The frequency synthesizer drives the Exciter section of the transmitter and provides a local oscillator (LO) signal to the superheterodyne receiver. The synthesizer, operates from 520.5 to 575.00 MHz, that is 1/2 of the transmitters frequency range of 1041 through 1150 MHz.

The basic frequency of the ÷N digital synthesizer is controlled by the 4 microsecond (0.25 MHz) reference pulses from U302, the output frequency, however, is remotely selected via the NAV receiver.

The calibrations of the channel selections are 108.00 through 117.95 MHz, the VHF frequencies of the paired VOR/DME channels. The actual paired DME transmit frequencies are 1041 through 1150 MHz. Table 4.1 provides paired frequency versus VCO frequency information. When the pilot sets his frequency controls, the synthesizer logic produces a VCO control voltage that sets the VCO to the required operating frequency for that channel. The control voltage applied to voltage variable capacitor CR401 determines what its effective capacitance will be. This capacitor and C402 are series connected across L401 to form a tank circuit that determines the frequency of the VCO.

The following describes synthesizer operation when channel 116.9 MHz (see Table 4.1: 116 X = VOR 116.9-- transmitter 1140 MHz, synthesizer 570 MHz) is selected by the NAV. Refer to VCO/SYNTH schematic and Figures 4-11 and 4-12.

TABLE 4.8. ARINC TO SYNTHESIZER CODE CONVERSION

MHz	ARINC				Output from U402				KHz	ARINC				Output from U402			
	A	B	C	D	A8	A4	A2	A1		A	B	C	D	B8	B4	B2	B1
108	0	X	X	0	X	0	0	X	.0	X	0	X	X	X	0	0	X
109	0	X	X	X	X	0	0	0	.1	0	0	X	X	X	0	0	0
110	X	0	X	X	0	X	X	X	.2	0	X	0	X	0	X	X	X
111	0	0	X	X	0	X	X	0	.3	X	0	0	X	0	X	X	0
112(.0/.2)	0	X	0	X	0	X	0	X	.4	X	0	X	0	0	X	0	X
112(.3/.9)	0	X	0	X	0	X	0	0	.5	X	X	0	0	0	X	0	0
113	X	0	0	X	0	0	X	X	.6	X	X	0	X	0	0	X	X
114	X	0	X	0	0	0	X	0	.7	X	X	X	0	0	0	X	0
115	X	X	0	0	0	0	0	X	.8	0	X	X	0	0	0	0	X
116	X	X	0	X	0	0	0	0	.9	0	X	X	X	0	0	0	0
117	X	X	X	0	X	X	X	X									

X= LOGIC HIGH 0= LOGIC LOW

Dwg. No. TP00910

4.8.8 Continued

The VCO is locked at 570 MHz, 1/2 the transmitted frequency, by the VCO control voltage obtained from the logic. The 570 MHz frequency is connected through buffer Q402 to RF amplifier Q403, into a ÷2 prescaler. The prescaler is a push-pull oscillator comprised of Q404, Q405 and L406. With the 570 MHz input the prescaler output is 285 MHz and is fed to the ÷N counter chain. For the example chosen, "N" is equal to 1140.

The remote channeling lines are not in binary form, they are in the ARINC 2/5 code form. Additionally, there is an 11 MHz transmitter output frequency jump between 112.2 and 112.3 MHz. A code conversion is required to change the ARINC code to the required Binary format. The microprocessor is programmed to provide this code conversion. Table 4.8 shows the input to output code.

Continuing the example, 116.9 MHz was chosen. When this frequency is set, the microprocessor will send a channel clock and serial data to U402, a serial in/parallel out shift register. This data and clock is sent only one time per frequency selection. Note in Table 4.8 that the MHz code lines (A8, A4, A2, A1) from U402 are all logic LOW as are the KHz code lines (B8, B4, B2, B1). These data lines are connected to the inputs of U404, U405, and U406, that are 4 bit high speed binary counters that count by 16.

The 285 MHz from the ÷2 prescaler is capacitive coupled into U401, an ECL 11C90 650 MHz ÷10/11 prescaler. The Mode Control (M2 pin 3) input controls the count sequence. A logic HIGH to M2 sets U401 in the ÷10 mode while a logic LOW sets it to a ÷11 sequence. The output from U401, (QTT_L pin 11) serves as a clock for the 4 bit counters, U404, U405 and U406.

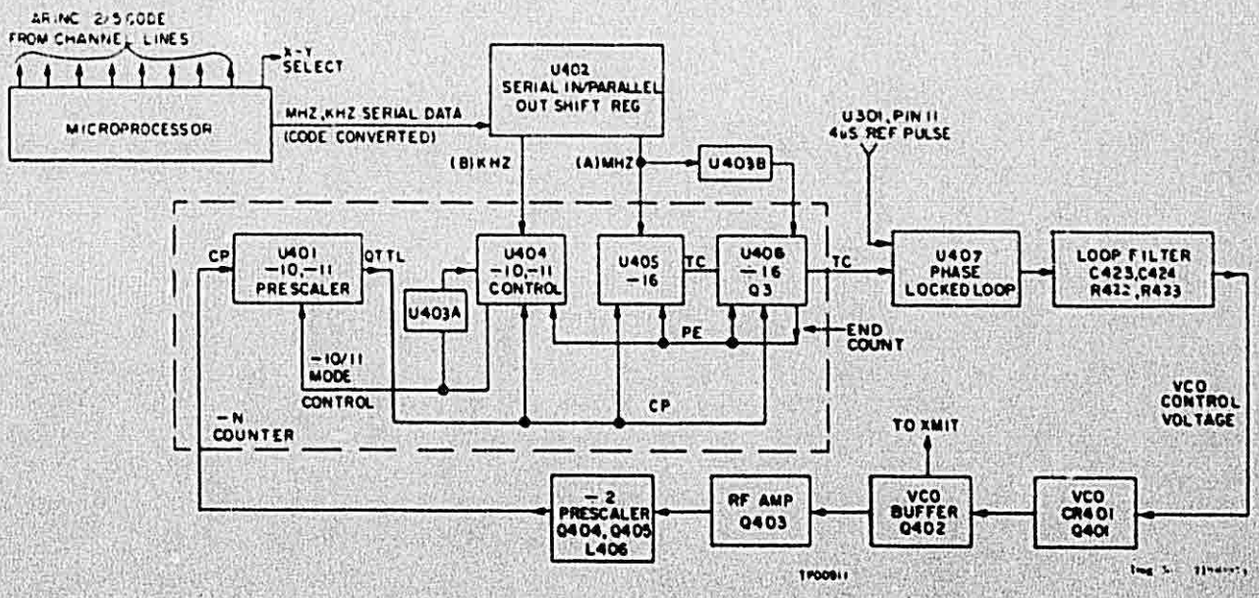


FIGURE 4-11. SYNTHESIZER BLOCK DIAGRAM

4.8.8 Continued

When the ÷N counter has reached its end count, Q3 (pin 11) of U406 goes logic LOW. Q3 is connected to the parallel enable (PE) inputs of U404, U405, U406. When the PE input is logic HIGH the counters are set in the Count Mode, when PE is logic LOW, the counters are set in the Load Sequence. In our example, the ÷N number is 1140 and the count sequence will begin after the counters are loaded. Refer to Figure 4-12.

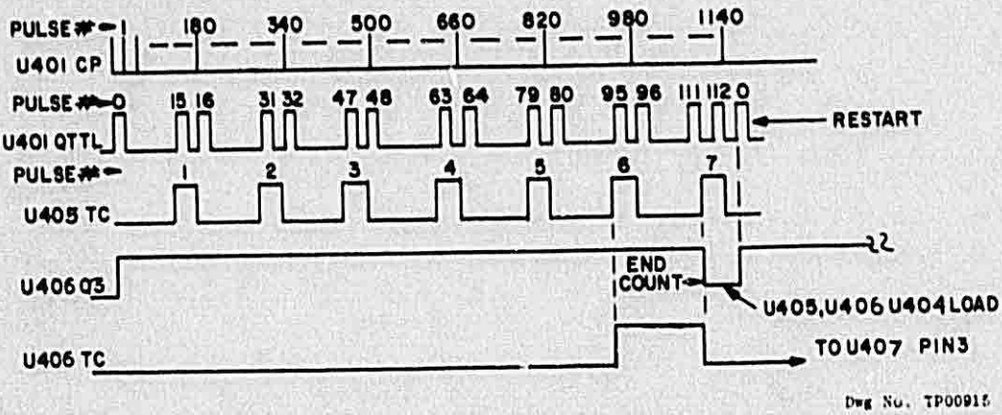


FIGURE 4-12. SYNTHESIZER DIGITAL TIMING FOR 116.90 MHz

When Q3 of U406 goes logic LOW, upon a receipt of the next clock pulse from U401, the data at the inputs to the counters are transferred to the outputs. KHz lines B8 to B1 and MHz lines A8 to A1 are logic LOW. MHz lines A8 to A4 are connected to NAND gate U403B which inverts the inputs and gives a logic HIGH to PO (pin 3) of U406. Note that P1 and P2 are tied to ground and P3 binary is tied to +5 volts. This presets the inputs of U406 to the binary number 9 (1001). Therefore this counter only needs to count from 9 to 16 to finish its count.

When the inputs are transferred to the outputs, Q3 of U406 goes logic HIGH and sets the counters to the Count Mode. Q3 and Q1 of U404 go logic LOW. This is inverted by NAND gate U403A and sets the Count Enable Parallel (CEP) to logic HIGH which enables U404. The logic LOW at Q3 and Q1 will pull the junction of R416, R417, and R418 to logic LOW which sets U401 (M2 pin 3) in the ÷11 count mode. Note that the Count Enable Parallel (CEP pin 7) input to U406 is tied to the Terminal Count (TC pin 15) output of Q405. A logic HIGH to a CEP will enable the counter while a logic LOW input will put the counter in the "HOLD" mode, freezing the outputs at the state prior to the HOLD command. A TC output is a fully decoded output and will go logic HIGH on the count of 15 and return to logic LOW on the 16th count. Since U406 only needs to count from 9 (preset) to 16, it will require 7 TC pulses from U405 to enable it to complete its count.

4.8.8 Continued

As the count begins, the 285 MHz pulses into U401 are being divided by 11. The Q3 (÷16) and Q1 (÷4) outputs are connected to NAND gate U403A and when both are logic HIGH, the output of U403A goes logic LOW, freezing (HOLD) the counter U404. The logic HIGH at Q1 and Q3 allows the junction of R416/R417/R418 to rise to +5 volts which now sets U401 in the ÷10 mode. U401 is now locked in the ÷10 mode for the rest of the count. At this point in time note that 120 of the 285 MHz pulses have been counted and U401 has put out 11 clock pulses. On the 15th clock pulse from U401, the TC (pin 15) output of U405 goes HIGH and on the 16th clock pulse goes LOW.

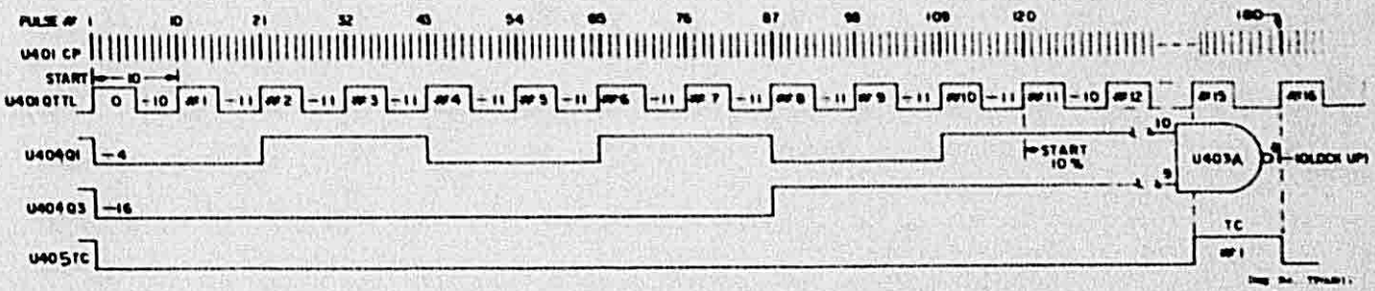


FIGURE 4-13. ÷10/11 MODE CONTROL SEQUENCE

This is the first of 7 TC pulses needed by U406 to complete its count. At this point in time, 180 of the 258 MHz pulses have been counted. Since U401 is now dividing by 10, it will take 160 of the 285 MHz pulses to give a TC output. Since 6 TC pulses are still needed, then 960 (160 X 6) of the 285 MHz pulses are required to complete the count. The total number of pulses counted will be 1140 (180 pulses for the first TC + 960 pulses for 6 more TC pulses). On the 1140th pulse, Q3 of U406 goes LOW, commanding the counters to LOAD and count sequence will begin again.

The decoded TC output from U406 is applied to the Phase Comparator B (PCB pin 3) input of the phase locked loop, U407. In addition, a 4 microsecond (.25 MHz) reference is applied to the Phase Comparator A (PCA) input. If any difference in frequency exists (out-of-lock mode), the comparison of this 4 us clock against the divided down VCO frequency produces an error signal from the Phase Comparator 2 (PC2 pin 13) output. The error signal is filtered by C423, R422, R423, and C424 and applied to Varicap CR401 that controls the frequency of the VCO. This closed loop causes the output (TC) of U406 (in-lock-mode) to be a 4 us repetitious waveform into the PCB input of U407.

4.8.8 Continued

Referring to the VCO/SYNTH Schematic, the VCO has two output paths. The first path is through L401, L402 and buffer Q402. The direct high-level output of the buffer, through impedance matching inductor L403, serves as an excitation of approximately +2 dBm into the exciter section of the transmitter. The purpose of inductor L404 is to parallel resonate with the parasitic capacity of Q402 that raises the impedance at the collector.

The second path is from the buffer Q402 into the RF Amplifier Q403. The gain of the amplifier is approximately 20 dBm. L405 is used to parallel resonate the parasitic capacity of Q403. The output of Q403 is coupled into the ÷2 oscillator through capacitor C414 and serves to lock the oscillator to 1/2 the VCO frequency.

Q404 and Q405 act as a push-pull oscillator that will run free at some frequency near the center of the band (270 MHz). Circuit operation is as follows: Inductor L407 is a high impedance to the 270 MHz and a DC return path for the biasing network. Current drawn through L407 passes through diodes CR402 and CR403, resistors R411 and R413, and also through resistors R408 and R415, back to -14 volts. This establishes approximately -5.5 volts at the junction of R409 and R413 that is the common bias line for all the transistors in the VCO chain.

Inductor L406 has a parasitic capacity distributed across its windings which forms a tank circuit in the collectors of Q404 and Q405 whose resonant frequency is 270 MHz. Because of dissimilar Betas (hFe) in Q404 and Q405, one will turn on before the other. Assume that Q404 turns on first. The collector of Q404 is pulled down toward -14 volts and the parasitic capacitor across L406 begins to charge toward -14 volts. Initially, the rate of change or charging current generates an EMF in L406. When the charging current drops off to the steady state (quiescent), the stored energy in the inductor collapses and generates a counter EMF at the junction of L406 and L407. This negative voltage transition back biases CR404 and is coupled through the parasitic capacitor associated with this diode and turns off Q404. As the magnetic field in L406 is collapsing, the collector ofQ404 falls back toward ground potential. When Q404 is turned off, Q405 turns on and repeats the sequence. The VCO frequency (550 MHz) is coupled into the common emitters and locks the oscillator to 1/2 the VCO frequency.

Capacitor C416 (across L407) is used to balance the oscillator coil, L406, as the other side of L406 is capacitive coupled into the ÷10/11 prescaler, U401.

4.9 Power Supply

The power requirements for the IDME 891 are met by a switching regulator (U801, Q801, T801) and a three terminal 8V regulator (U408).

The switching regulator provides the following output voltages:

1. -14V for the Synthesizer/VCO PC board
2. +60V for the transmitter modulator
3. +14V for the transmitter IF received and 3-terminal 8V regulator
4. + 5V for the Synthesizer/VCO, Interconnect PC board, and Range PC board

4.9.1 Switching Regulator

Refer to Figure 4-14 for the following discussion:

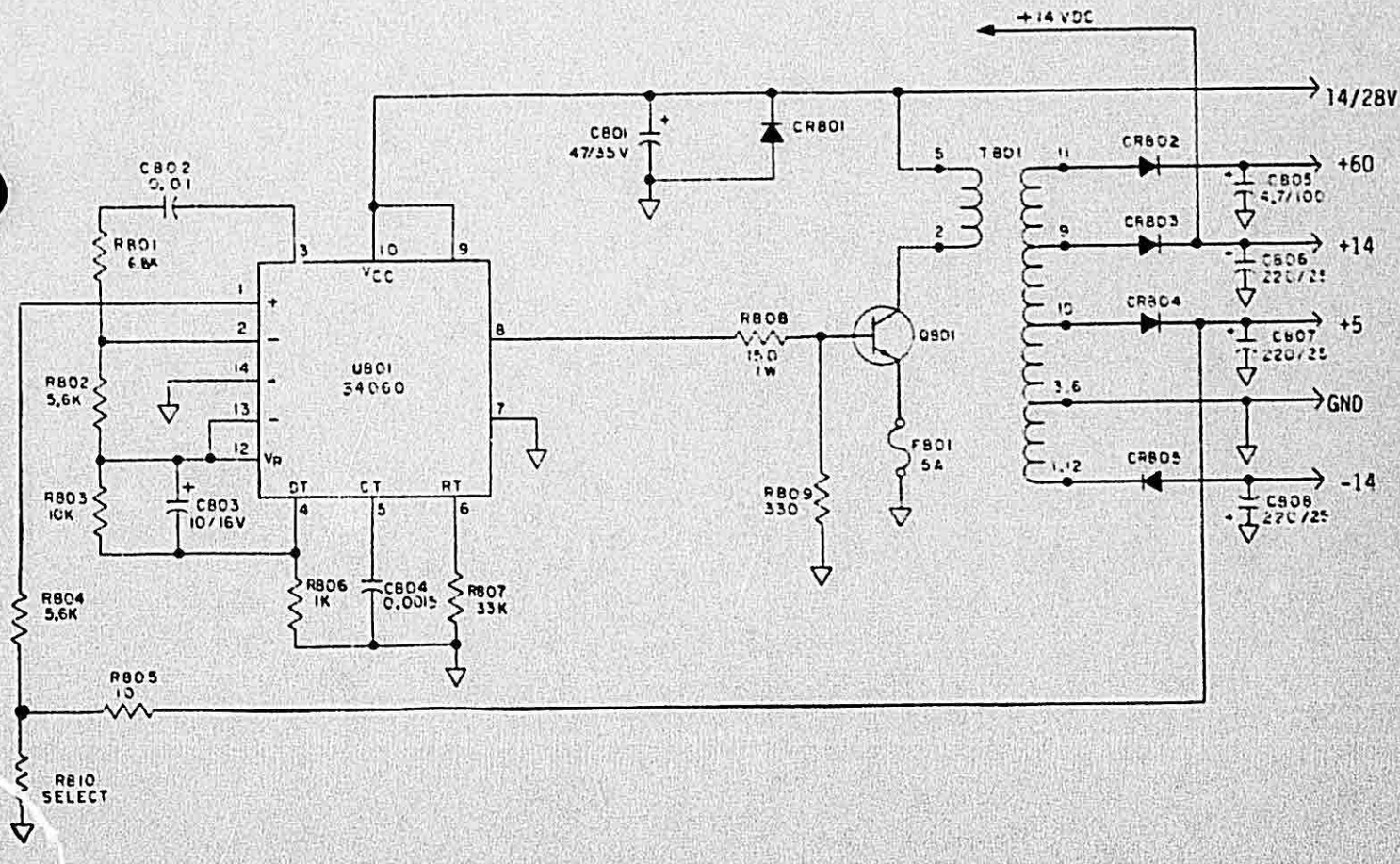


FIGURE 4-14. PULSE WIDTH MODULATED FLYBACK CONVERTER

4.9.1 Continued

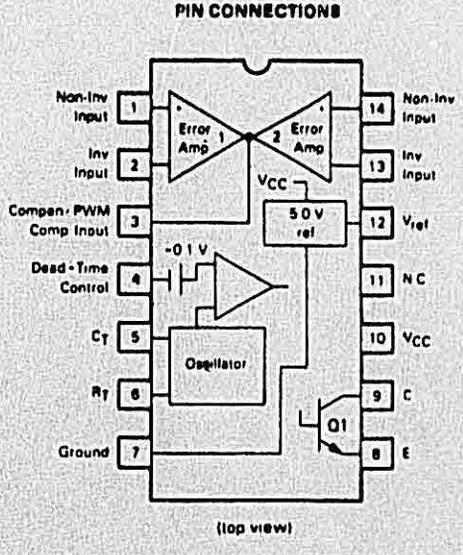
The switching regulator consists of pulse-width modulator U801, switching transistor Q801, transformer T801 and associated components. This design is called a "pulse-width modulated, soft start, flyback converter". It works by cyclically storing energy in a magnetic field and then delivering this stored energy to a load. The output voltages are controlled by varying the on to off ratio of switching transistor Q801. Therefore, output voltages depends on both the turns ratio of T801 and the on/off ratio of Q801 which is controlled by U801 (MC34060).

The operation of the flyback converter is different from a conventional transformer circuit because during the charge cycle the secondary or load is completely disconnected from the primary. Transformer's T801 secondary polarity is such that when Q801 is turned on, the anodes of CR802/803/804 and cathode of CR805 are reversed biased and the secondary is open-circuited. During the on time of Q801, storage capacitors C805/806/807/808 supply the total output current.

When Q801 turns off, the collapsing energy field of T801 reverses the polarity of the secondary windings which forward biases the diodes. The energy stored in the core is transferred into the load and storage capacitors, replenishing the capacitor's lost charge when Q801 was on.

4.9.2 The MC34060 Pulse-Width Modulator

This integrated circuit is a fixed frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 4-15)



4.9.2 Continued

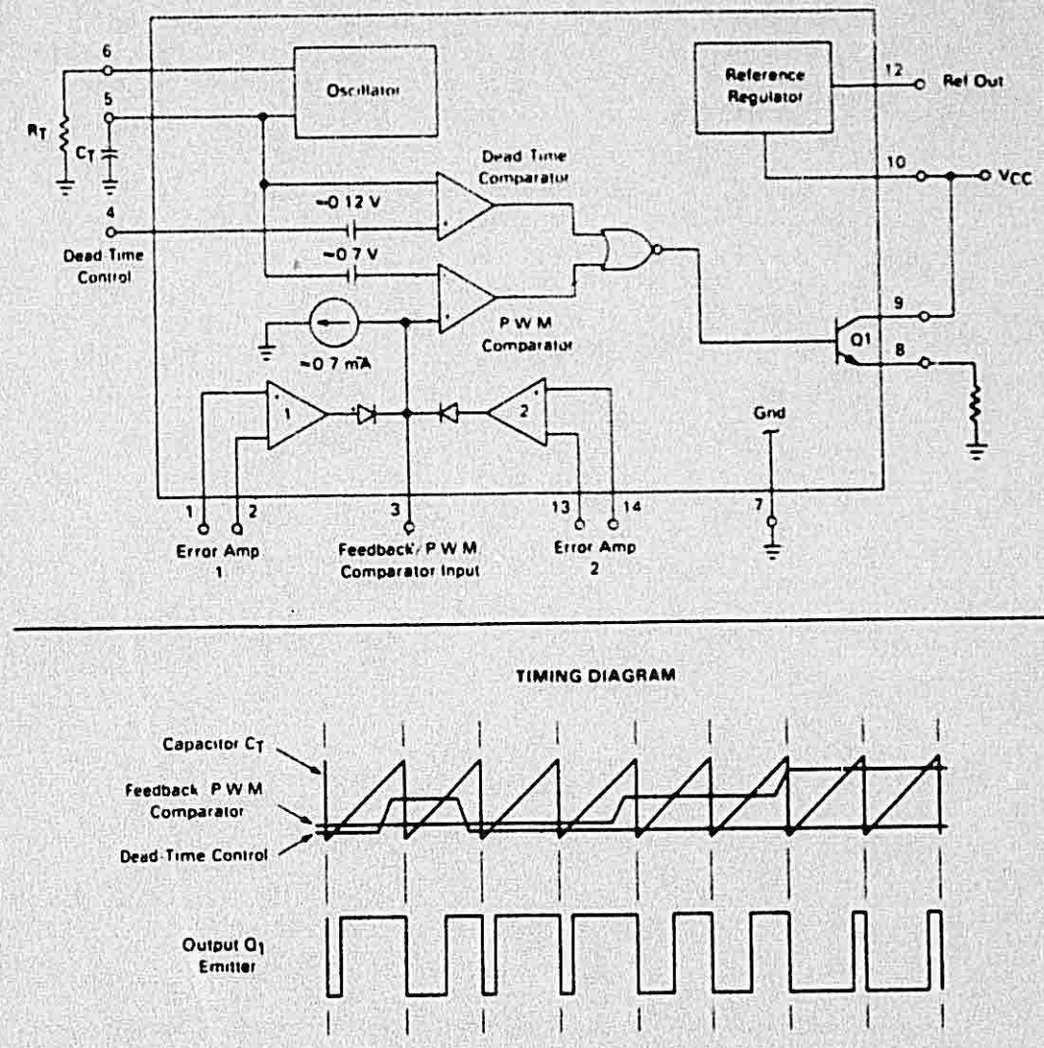


FIGURE 4-15. MC34060 PULSE WIDTH CONTROLLER

An internal linear sawtooth oscillator is frequency programmable by two external components CR807/C804). Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C804 to either of two control signals. The output is enabled only during that portion of time when the sawtooth is greater than the control signals. Therefore, an increase in control signal amplitude causes a corresponding linear decrease of output pulse width. (See timing diagram in Figure 4-15)

4.9.2 Continued

The control signals are external inputs that can be fed into the dead-time (DT) control, the error amplifier inputs, or the feedback (pin 3) input. The dead-time control comparator has an effective 120 millivolt input off-set which limits the minimum output dead-time (OFF) to the first 4% of the sawtooth cycle time. This would result in a maximum output pulse duty cycle of 96%. However, additional dead time (75%) is imposed on the output by the external resistors R803/R806. (See Figure 4-14) The internal pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead-time control input, down to zero, as the voltage at the feedback pin 3 varies from 0.5 to 3.5 V.

Error amplifier number 2 (pins 13/14) is not used and is biased off by grounding pin 14 and applying 5 volts (V REF) to pin 13. Error amplifier number 1 is used to sense the output 5 volt line by comparing the internal 5 volt (V REF) present at pin 2 via R802 to the 5 volt output applied to pin 1 via resistors R804/R805.

The error amplifiers outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. If the 5 volt output line increases, error amplifier number 1 will amplify this increase and cause the PWM comparator to go logic HIGH. This causes the duty cycle of the pulse applied to Q801 to decrease, thereby lowering the 5 volt output from T801.

The operating frequency of U801 is approximately 22 KHz and is determined by capacitor C804 and resistor R807.

4.10 L.E.D. DISPLAY

The DME display consists of four 7-segment light emitting diodes (L.E.D.). The display normally provides distance information in nautical miles (NM) with a resolution of 0.1 NM. When the front panel OBS Knob is pushed in and held in the display information is the aircraft's ground speed in nautical miles per hour (KTS) with a resolution of 1 KT.

A decimal point is located in digit #3 and is always operating in the distance mode. When in the velocity mode, the decimal point is always extinguished.

When the distance is below one hundred miles, the hundred numeral in digit #1 is blank, when below ten miles digit #2 is blank.

A "bar" readout in the Display, indicating a fault, will be seen by the illumination of the "G" segment of digits #2, #3 and #4. Digit #1 will be blank during a fault as this digit can only display the number "1" (segments b and c).

4.10.1 Display Theory of Operation

Refer to the Range Board Schematic in Section 6 for the following discussion:

When the search/track counter (U303, U304, U305) reaches its end count, a pulse from Q3 of U305 called the external interrupt pulse is applied to pin 38 of the microprocessor. Since the search/track counter runs continuously, there is a steady stream of external interrupt pulses applied to microprocessor. Each pulse signals the microprocessor to encode the 7-segment output lines and select which of the four digits is to be illuminated.

The segment output lines are applied directly to three octal D type flip-flops identified as Latch A (U501), Latch B (U503) and Latch C (U505) (see Bottom Interconnect Board Schematic). The logic state of the segment lines will be transferred to the latch outputs upon receipt of a latch clock pulse. The latch outputs are applied to segment drivers U502 which drives digits 1 and 2, U504 which drives digit 3 and U506 which drives digit 4.

The latch clock pulses are not synchronized so that all four digits are simultaneously energized; rather they are timed to give a Latch A, Latch B, Latch C sequence. The segment lines are being encoded by the microprocessor to give both distance and velocity information. The DME display normally shows distance information. The microprocessor synchronizes the Latch A clock pulse to be time coincident with the segment lines that contain the distance information for digits 1 and 2. It next synchronizes the Latch B clock with segment distance information for digit 3 and last, it syncronizes Latch C clock with distance information for digit 4. The segment lines containing velocity information will not be time coincident with the Latch clock pulses which are normally timed for the distance information, therefore velocy cannot be displayed. If velocity information is desired, then the Latch A, B, C clock pulses must be shifted to be time coincident with segment line velocity information.

The generation of the Latch A, B, C clock pulses is accomplished by U314, a 1-of-8 decoder and U315, a quad 2-input multiplexer. For every external interrupt pulse applied to U313-38 (uP) an E2 enable pulse is issued from U313-7 and applied to pin 5 (E2) of U314. The E1 (pin 4) input of U314 is tied to ground and the E3 (pin 6) input is tied to 5 volts. According to the truth table in Figure 4-16, when E2 pulse is high, irregardless of the A0, A1, A2 select inputs, all Q outputs of U314 are forced high. When E2 pulse goes low, then the A0, A1, A2 select inputs from the microprocessor will determine which Q output will go low. The Q0, Q1, Q2 outputs from U314 are the Latch A, B. C distance mode clocks.

The Q3, Q4, Q5 outputs from U314 are the Latch A, B, C velocity mode clocks. The timing diagram of Figure 4-16 shows how the A0, A1, A2 select input pulses from the microprocessor generates the Latch clock

4.10.1 Continued

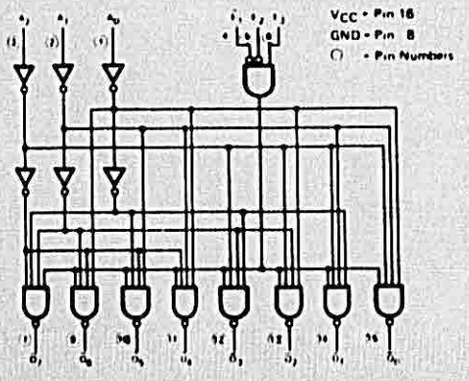
pulses. Note that the first pulse generated is a Latch A distance mode clock pulse, the second is a Latch A velocity mode clock pulse, followed by the Latch B and C distance and velocity mode clock pulses.

All the Latch clock pulses are applied to the inputs of U315, a Quad 2-input multiplexer. There are six inputs to U315 but only three outputs. Pin 1 of U315 is a select control input. Pin 1 is pulled up to 5 volts thru resistor R340 and is also connected to a switch which is controlled by the front panel OBS knob. When the OBS knob is pushed in, the switch grounds pin 1. Since pin 1 is normally at 5 volts, this constitutes the normal distance mode of operation. When 5 volts is applied to U315-1, then U315 will transfer the Q0, Q1, and Q2 outputs of U314 to its three outputs at pins 4, 7 and 9 while inhibiting all other inputs. These three outputs now become the Latch A, B, C distance mode clock pulses.

When the OBS knob is pushed in and U315-1 is grounded, then U315 will transfer the Q3, Q4, and Q5 outputs of U314 to its three outputs. These become the Latch A, B, C velocity mode clock pulses. Figure 4-16 shows the timing shift between a distance and velocity clock pulse which is necessary in order to achieve time coincidence with the segment distance or velocity information.

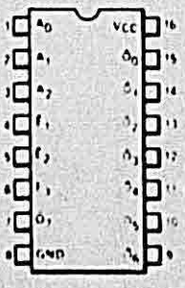
The outputs from Latches A, B and C drive Darlington Transistor Arrays (U501, U503, U505) whose outputs are uncommitted collectors of transistors. Each collector is tied to a segment output of an L.E.D. in the display. When the Darlington transistor is turned on, the collector is grounded and current sinks the segment line of the L.E.D. which illuminates the segment.

LOGIC DIAGRAM



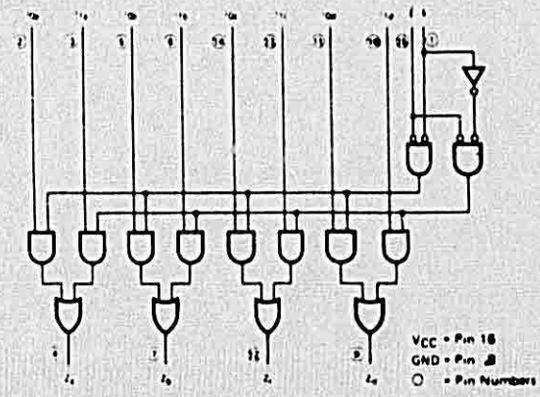
PIN NAMES

$A_0 - A_2$	Address Inputs
$\bar{E}_1, \bar{E}_2$	Enable (Active LOW) Inputs
E_3	Enable (Active HIGH) Input
$\bar{O}_0 - \bar{O}_7$	Active LOW Outputs



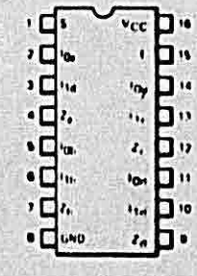
U314 74HC138

LOGIC DIAGRAM



PIN NAMES

S	Common Select Input
$\bar{E}$	Enable (Active LOW) Input
$I_{0a} - I_{0d}$	Data Inputs from Source 0
$I_{1a} - I_{1d}$	Data Inputs from Source 1
$Z_a - Z_d$	Multiplexer Outputs (Note b)



U315 74HC157

4.10.1 Continued

TRUTH TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	E_3	A_0	A_1	A_2	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

U314 74HC138

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\bar{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

U315 74HC157

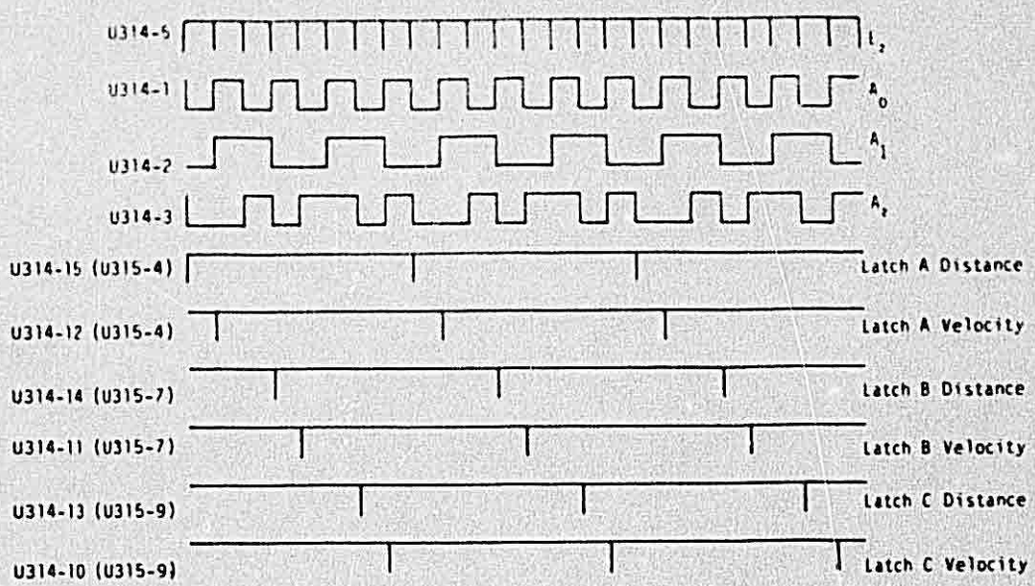


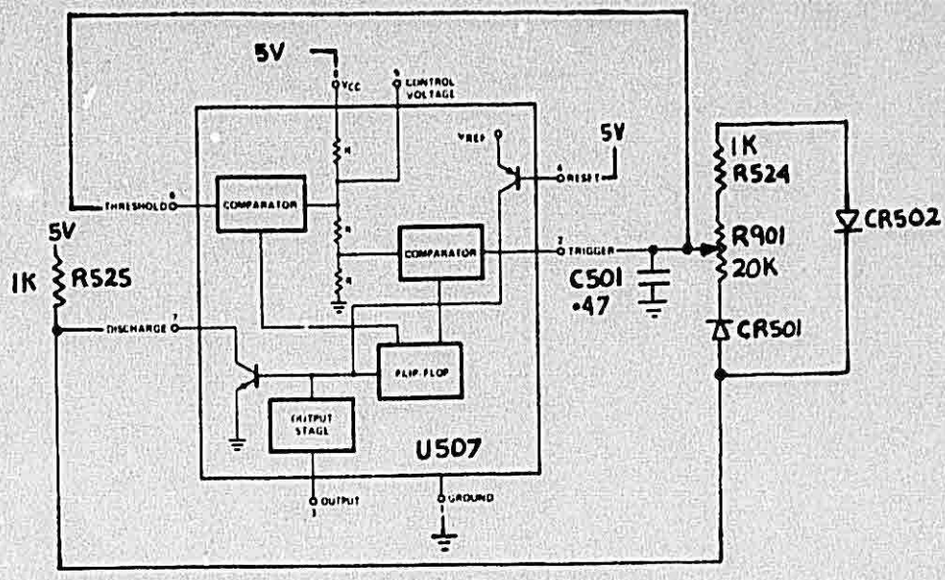
FIGURE 4-16. LATCH A, B, C CLOCK TIMING DIAGRAM

4.10.2 Display Dimmer

Display intensity is manually controlled by a potentiometer which is part of the front panel ON/OFF switch.

The dimmer circuit consists of a 555 Timer (U507) connected as an Astable (free running) multivibrator. A block diagram of the 555 Timer is shown here. Refer to the Bottom Interconnect Board Schematic for the following discussion.

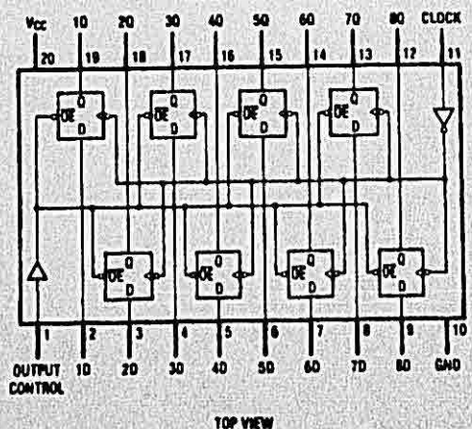
4.10.2 Continued



555 TIMER BLOCK DIAGRAM

In this design, U507-2 (trigger) and U507-6 (threshold) are tied together for self triggering. Capacitor C501 tied to pins 2 and 6 charges thru R525, CR501 and a portion of R901, the front panel dimmer control potentiometer. When the charge on C501 reaches 2/3 of the 5 volt (Vcc) supply, the internal comparator at pin 6 will trip and reset the internal flip-flop which turns on the internal transistor connected to pin 7. The flip-flop also drives the output at pin 3 high. The charge on capacitor C501 will discharge thru a portion of R901, R524 and CR 502 back to ground thru the transistor at pin 7. When the charge on C501 drops to 1/3 of the 5 volt (Vcc) supply, the compartor at pin 6 will set the internal flip-flop which turns off the internal discharge transistor and also drives the output (pin 3) low. Thus it can be seen that the ratio of the total charging resistance to the discharging resistance will determine the duty cycle of the output, This ratio (duty cycle) can be varied according to the setting of R901, the dimmer pot.

The output from U507-3 is simultaneously applied to pin 1 of U501, U503 and U505, the segment Latches. A logic high at the Latch pin 1 will set the Latch outputs to a high impedance state which turns off the segment drivers U502, U504 and U506. Thus, display dimming action is directly proportional to the duty cycle output from the 555 Timer.



TOP VIEW

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

LATCHES U501,U503,U505

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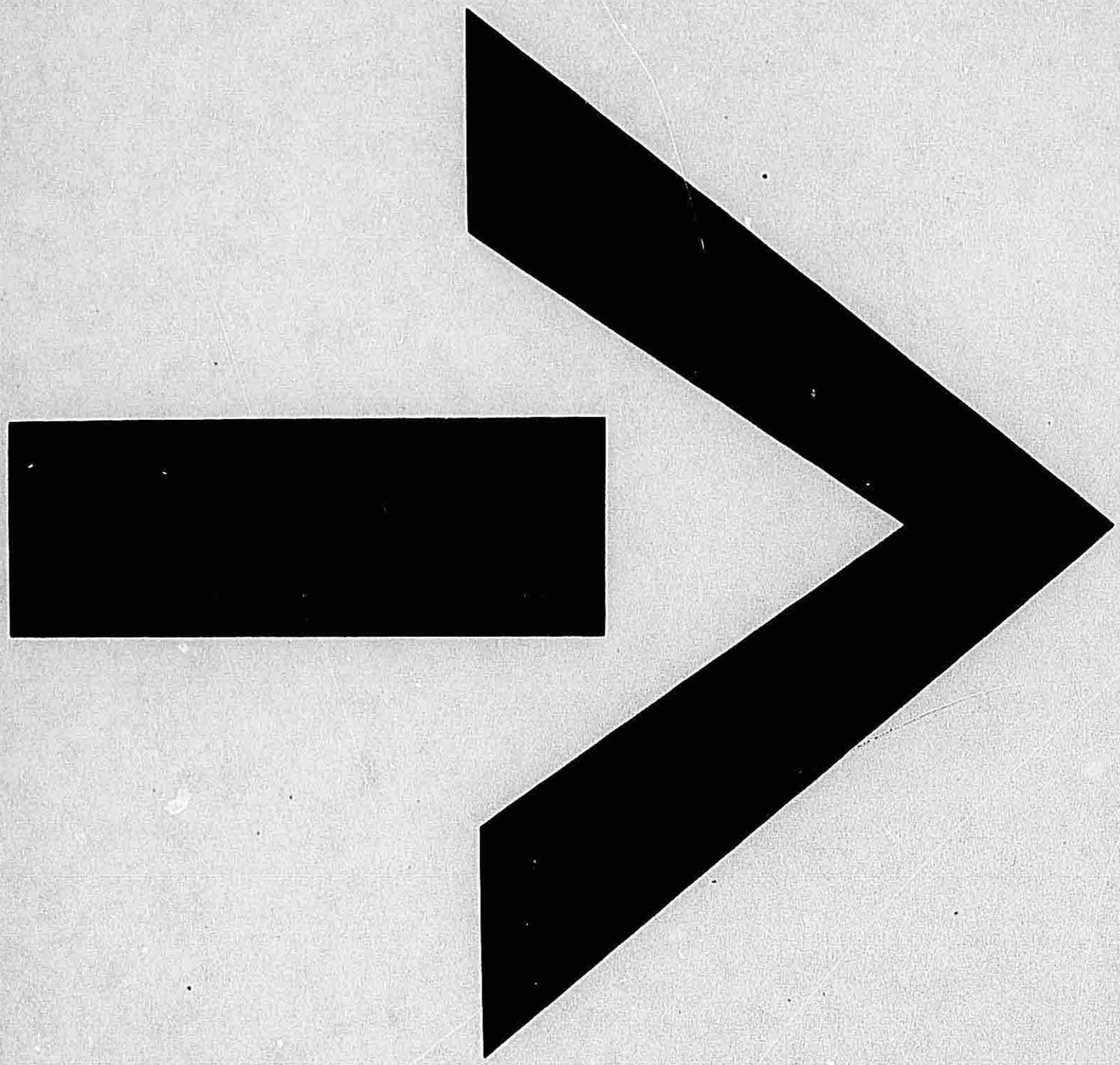
LIST OF ILLUSTRATIONS



5.1 INTRODUCTION

This section provides instructions for the corrective maintenance of the IDME 891. The performance characteristics given in Section 5.4 provide a series of tests for the DME circuits and VOR-ILS indicator. If these results cannot be obtained then either the alignment or troubleshooting procedures should be consulted in order to correct the fault.

5.2 MODULE EXCHANGE PROGRAM

The following complete and tested modules are available on an exchange basis:

PART NUMBER	DESCRIPTION
01426-1390	VCO/SYNTHESIZER PC BOARD MODULE
01427-1390	IF RECEIVER/POWER SUPPLY PC BOARD MODULE
01423-1390	TRANSMITTER/EXCITER ASSEMBLY

5.3 TEST EQUIPMENT REQUIREMENTS

A list of recommended test equipment used for alignment and troubleshooting is shown here. Any test equipment having similar characteristics may be substituted.

TYPE	CHARACTERISTIC	EXAMPLE
DC Power Supply	Voltage Range: 0-30 VDC Current Range: 0-1 AMP.	Power Designs MODEL 5015
DME Generator	- - - - - - - - - - - - - -	IFR 1200Y3
Oscilloscope	- - - - - - - - - - - - - -	TexTronix MODEL 535
Digital Voltmeter	DC Ranges: Input impedance 10 Meg. Min 0.001 to 100 Volts Accuracy 2% of range AC Ranges: Input impedance 1 Meg. Min 0.01 to 100 Vrms Frequency 10 HZ-1 Mhz Accuracy 2%	SIMPSON MODEL 460
RF Power Meter	- - - - - - - - - - - - - -	H.P. MODEL 431B
Frequency Counter	600 Mhz range	FLUKE MODEL 1912A

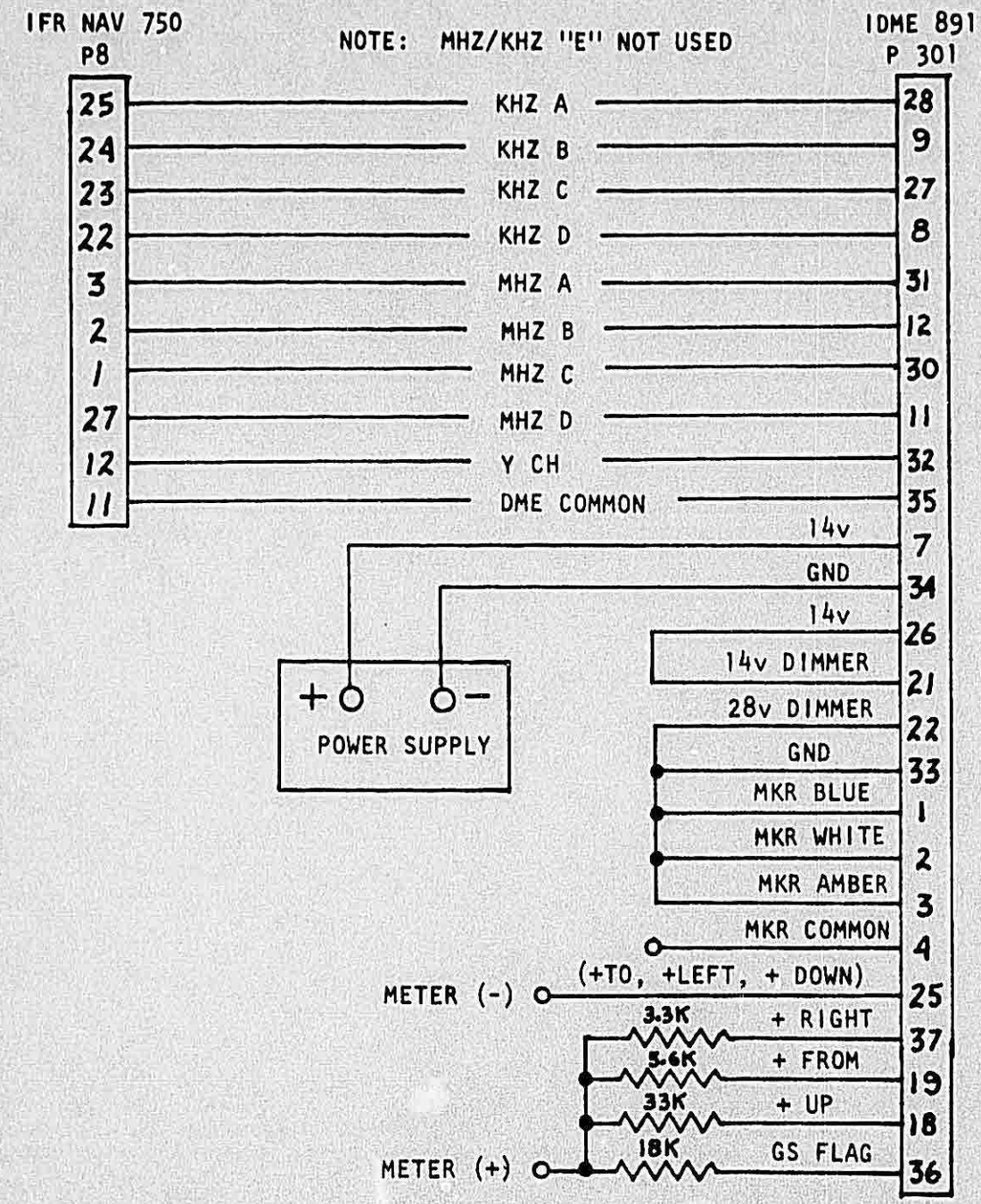


FIGURE 5-1 BENCH TEST HARNESS

5.4 PERFORMANCE TESTS

Before conducting the Performance test, refer to Section 3 (OPERATION) to familiarize yourself with the IDME 891 operation.

The following test is conducted with a harness constructed as shown in Figure 5-1.

A. DME SECTION TEST

1. Turn IDME 891 power switch to OFF position.
2. Connect system for bench test as shown in Figure 5-1.
3. Set the DME test generator parameters as follows:

   RANGE: 100 nm.
   ATTENUATOR: -73 dBm
   REPLY EFFICIENCY: 70%
   SQUITTER: 2700
   FREQUENCY: 112.50 MHz
   IDENT: ON

4. Channel the IFR NAV 750 to 112.50 MHz.
5. Set the power supply to 14 Vdc.
6. Turn the IDME 891 power switch to "ON" position.
7. Verify that the DME's distance readout is illuminated and reads 100 ±.2 nm.
8. Set the DME test generator groundspeed to 240 knots, direction inbound.
9. Set DME test generator range switch to "velocity" position.
10. Verify that the DME distance is smoothly tracking inbound in 0.1 nm steps.
11. Allow the groundspeed to stabilize a minimum of 5 minutes.
12. Check groundspeed by depressing the VOR course selector knob. The displayed groundspeed should be within ±5% of that indicated (240 kts) on the test generator.
13. Check sensitivity during tracking. IDME 891 should track at -82 dBm.
14. Remove the RF signal from the IDME 891. Verify that, in approximately 10 seconds, the DME readout displays BARS. Restore the RF signal.
15. Verify remote channeling of ALL KHz channels by checking for lock on as the IFR NAV 750 and DME test generator KHz frequency select switches are cycled from 0 to .95.
16. Verify remote channeling of ALL MHz channels as per Step 15.
17. Check the DME display dimming operation by rotating the dimmer control knob thru its full range.
18. Check transmitter power on all channels. Power should be 25W nominal.

    CAUTION: Many DME test generators do not have the capability to accurately measure power as low as 25 watts.

5.4 Continued

18. Continued

NOTE: The digital system of the IDME 891 operates statistically on a TACAN or DME signal. Some test generators do not accurately simulate the ground DME or TACAN signal and may not operate the IDME 891 correctly. The result is improper distance or groundspeed computation. This is usually caused when squitter or countdown is not produced in a random manner.

B. VOR-ILS INDICATOR SECTION TEST

1. Turn the IDME 891 power switch to the OFF position.
2. Reset the power supply to 5.5 Vdc.
3. LEFT/RIGHT, TO/FROM, UP/DOWN, GS FLAG TEST

a) Touch the Meter (-) lead to the power supply negative terminal and the Meter (+) lead to the positive (5.5 Vdc) terminal. Verify that the L/R needle deflects 5 dots to the right, the T/F flag displays a full FROM, the GS UP/DN needle deflects full down to the bottom bar and the GS Flag retracts fully from view.

b) Reverse the Meter (+) and (-) leads at the power supply and verify that the GS Flag is in full view, the L/R needle deflects 5 dots to the left, the T/F flag displays a full "TO", the GS UP/DN needle deflects full "UP" to the top bar.

5.5 ALIGNMENT AND ADJUSTMENT

5.5.1 Clock Generator Checkout and Adjustment

(a) Apply power to IDME 891.
(b) Connect frequency counter to crystal oscillator output U310D pin 8.
(c) Frequency should be 4.000000 ±100 Hz (+4.000100, -3,999900).
(d) If frequency is not within these limits, change value of capacitor C319 to obtain correct clock frequency.

5.5.2 Synthesizer Checkout and Adjustment

The frequency synthesizer checkout comprises a check of the VCO frequencies and power at J101, throughout the band. See Table 4.1 in Section 4 for a list of the VCO frequencies. The procedure for adjusting the VCO control voltage and power output is as follows:

(a) Connect frequency counter to VCO buffer output at J101.
(b) Set channel to 117.90 MHz. The frequency counter reading shall be 575.0 MHz ±50 ppm* (28.75 KHz).

5.5.2 Continued

(c) Connect a digital voltmeter to VCO control line (junction of R422/R423). Voltage should be 7.2 ±0.3 Vdc.
(d) Set channel switch to 108.00 MHz. The frequency shall be 520.5 MHz ±50 ppm* (26.03 KHz).
(e) The VCO voltage should not be less than 0.6 Vdc.
(f) If the VCO voltages are out of tolerance at 117.9 and 108.00, set the channel to 117.90 MHz. Adjust L401 for 7.2 Vdc ±0.3 Vdc.
(g) Power Adjustment:
Connect RF milliwattmeter to J101.
Adjust L402 for 2.0 ±1 mw across the band.

* parts per million - ie: Tolerance X Frequency = Hz
50 X 575.0 = 28,750 Hz = 28.75 KHz

5.5.3 RF Transmitter Pulse Width Measurement and Adjustment

The transmitter pulse width is factory aligned and normally does not require field alignment. However, transmitter or modulator circuit problems that require the replacing of circuit components may necessitate a transmitter pulse width adjustment. The procedure for measurement and adjustment is given below:

(a) Set the DME channel to 117.5 MHz.
(b) Monitor the detected transmitter pulse pair on an oscilloscope.
(c) Measure the transmitter pulse width at the 50% point of the pulses.
(d) Pulse width should be 3.5 ±0.5 us.
(e) If adjustment is required, adjust width with R331 located on the range board.

5.5.4 Dead Time Measurement and Adjustment

(a) Connect an oscilloscope to U308B-5.
(b) Make the following settings on the DME Signal generator:
1. Turn squitter off
2. Set reply efficiency to 100%
3. Set Mode Switch to "Range"
4. Set Distance to 5 nm
5. Set Attenuator to 78 dBm
6. Turn IDENT off
7. Trigger to "EXT"
(c) Pulse width should be 70 us ±5 us.
(d) If adjustment is required, adjust width with R335 located on the range board.

5.5.5 RF Alignment

The alignment procedures are provided as a method of checking the tuning of RF circuits in the IDME 891 after circuit components (RF transistors, capacitors) have been changed.

5.5.5.1 63 MHz IF Receiver Alignment

In the IF alignment, L704 through L709 are tuned by adjusting the coil's cores (slug), to provide a maximum detected pulse level.

The cores can be rotated for tuning, however, after tuning in and out for a peak many times, this excessive core movement will loosen the fit of the threads in the coil's body and thus the coil can become sensitive to vibration. If the core becomes loose, it should be removed, a single strand of lacing cord or equivalent inserted into the coil's body and then replace the core (and adjust). Under no conditions should cement be used to secure the core.

Procedure:

(a) Connect the IDME 891 for a standard bench test.
(b) Connect a scope probe to the collector of Q703. The cover over the top of the IF strip must be removed.
(c) Set the DME Signal Generator output attenuator to produce a 1 volt peak-to-peak pulse pair.
(d) Tune L704 through L709 and as the tuning progresses, reduce the DME Signal Generator's RF level to maintain a 1 volt peak-to-peak pulse pair.
(e) Reinstall the cover.

5.5.5.2 RF Transmitter Exciter Alignment

If an RF transistor or capacitor has been changed in the transmitter, the following procedure should be used to check proper operation and realign the repaired stage.

NOTE: Either the IDME 891's synthesizer, if operating properly, or an RF Signal Generator may be used. All steps using Generator are enclosed in parenthesis ().

(a) Set IDME 891 to 112.5 MHz.
(Connect the RF Signal Generator to P101, set generator frequency to 550 MHz CW and output attenuator to +3 dBm.)
(b) Using a 27K isolation resistor, connect a VTVM to the base of Q205.
(c) If the exciter is working properly, the voltage will be approximately +0.2 Vdc.
(d) Disconnect P101.
(Reduce the Signal Generator level by 20 db.)
The voltage should rise to +1 Vdc. This shows that stages Q201 through Q204 are operating correctly.

5.5.5.2 Continued

(e) If one of the transistors, Q202 thru Q205 has been changed, the voltage in step "C" may be used to check alignment as follows:

1. Set the IDME 891 to 108.0 MHz. (Set the Signal Generator to 520 MHz at a +3 dMm level.)
2. Observe the voltage at the base of Q205.
3. Change the IDME 891 frequency to 117.9 MHz.
4. Observe the voltage at the base of Q205.
5. Both voltage readings should be approximately 0.2 Vdc or slightly less.
6. If at one frequency the voltage is considerably higher than the other, tune the coil associated with the changed component by spreading or compressing the coil.
7. By this means it is possible to equalize the voltage at Q205 at both ends of the band.

5.6 TEST REQUIRED AFTER MODULE REPLACEMENT

The following are the recommended checks to perform after replacing a module in the IDME 891. Only those checks pertaining to that module being replaced need be checked.

5.6.1 63 MHz IF Receiver Module

After replacing this module check "lock-on" sensitivity at high and low frequencies. It should be -82 dMm minimum. If this sensitivity checks OK, unit is operating properly. If lock-on is less than -82 dBm, listen to IDENT, adjust RF level if noisy. Retune IF coils L704 thru L709 for maximum IDENT volume.

5.6.2 Transmitter Module

Check only for proper pulse width and power output. If defective, return it to the factory for exchange.

5.6.3 VCO/SYNTH. Module

Check and align if necessary as outlined in Section 5.5.2.

5.7 MECHANICAL DISASSEMBLY

5.7.1 Case Removal (Refer to Figure 6-1)

(a) Remove the two #4 screws and washers that secure the case to the rear plate of the unit.
(b) Remove the four #2 slotted black flat head screws located around the periphery of the case, directly behind the bezel.
(c) Pull the case to the rear to remove it from the chassis frame.

5.7.2 VCO/SYNTHESIZER P.C. Board Removal

(a) Disconnect VCO co-axial cable connector P-101 from transmitter co-ax connector J101 and pull the VCO cable back thru its guide hole in the mid-plate assembly.
(b) Pull the printed circuit board straight up until the board is clear of its retainer guides located on the mid and rear plate assemblies.

5.7.3 IF Receiver/Power Supply P.C. Board Removal

(a) Disconnect receiver co-axial cable connector J103 from transmitter co-ax connector P103 and pull the receiver cable back thru its guide hole in the mid-plate assembly.
(b) Pull the printed circuit board straight up until the board is clear of its retainer guides located on the mid and rear plate assemblies.

5.7.4 Transmitter/Exciter Assembly Removal (Refer to Figure 6-1)

(a) Disconnect the VCO and Receiver co-axial cables connectors (P101/J101 and P103/J103) and pull the cables back thru their guide holes in the mid-plate assembly.
(b) Remove the two #4 screws that secure the transmitter to the rear plate assembly.
(c) Remove the two #4 screws that secure the transmitter to the mid-plate assembly and pull the assembly from the chassis as far as the five wires will permit.
(d) Unsolder the five wires from the assembly.

5.7.5 Pilot Lamp Replacement (Refer to Figure 6-3)

(a) Remove the two #2 screws (item 65) and one slotted screw (item 64) that secures the light block (item 66).
(b) Break RTV cement seal (frontof light block) that secures lamp to be replaced.
(c) Unsolder lamp leads at the terminals of the rear of the light block; remove blue filter and then the lamp.
(d) Insert new lamp and filter and resolder the leads.
(e) Use non-corrosive RTV to secure lamp and filter.
(f) Replace light block and secure, using screws previously removed.

5.7.6 Meter Replacement

Refer to Figure 6-3.

(a) Set the azimuth card to 80 degrees. Remove the OBS knob (item 1) and spacer (item 3).
(b) Remove four #4 screws (item 8) securing the bezel (item 7) to the front casting (item 16) and remove the bezel.
(c) Remove the two #2 screws (item 19) that secure the dial guide spring (item 18), and remove the dial guide.

5.7.6 Continued

(d) Remove the azimuth card (item 13).
(e) Remove the black dial guide (item 14).
(f) Remove the #4 screw (item 35) holding meter to bracket (item 44).
(g) Remove the #2 screw (item 73) that secures the marker light block (item 74) to the meter.
(h) Remove the #4 screw (item 53) holding meter to bracket (item 52).
(i) Unsolder meter leads from the range board.
(j) Slide meter out the front of the unit.
(k) Replace meter and reassemble by performing the above steps in reverse order.

CAUTION: When replacing the azimuth card be sure to position the "80" degree at the top where it was originally set as requested in step (a). If this is not done, then the azimuth card and OBS pot are out of alignment. If realignment is required, see Section 5.8.

5.7.7 Removal of Control Head Assembly from Mid Plate Assembly

Refer to Figure 6-3

(a) Remove #4 flat head screw (item 40) that secures the rear casting (item 49) to the mid-plate assembly.
(b) Remove the #4 screw (item 83) that holds the 2 inch long hexagonal spacer (item 33) to the mid-plate assembly.
(c) Remove the #4 screw (item 34) from the rear casting (item 49). This screw is located on the flat side of the casting (next to the OBS pot) and holds the casting to the mid-plate right angle tab.
(d) Remove the #4 screw (item 83) that holds the rear casting to the mid-plate. This screw is located just above the OBS pot's upper right hand mounting screw.
(e) Gently pull the control head from the mid-plate as far as the meter wires will allow.

5.7.8 OBS Shaft Replacement

Refer to Figure 6-3)

(a) Set the azimuth card to 80 degrees.
(b) Remove the control head from the mid-plate as described in Section 5.7.7.

CAUTION: DO NOT disturb OBS pot gear (item 81) as this will throw the azimuth card and OBS pot out of alignment. See Section 5.8 for realignment.

(c) Remove OBS knob (item 1) and spacer (item 3).
(d) Loosen set screws (item 2) on OBS driver gear (item 61).
(e) Remove #4 screw (item 55) and OBS shaft spring (item 54).

5.7.8 Continued

(f) Loosen set screw (item 51) found in the rear casting. This set screw places tension on the OBS shaft.
(g) Pull OBS shaft (item 47), and spacer (item 48) from the rear casting (item 49).
(h) Insert new OBS shaft with old spacer into the rear casting.
(i) Replace OBS shaft spring (item 54) and secure with original screw.
(j) Secure OBS driver gear (item 61) to shaft. Make sure the shaft is as far forward as the spacer will permit.
(k) Replace OBS knob and spacer.
(l) Retighten set screw (item 51) to put tension on shaft.
(m) Reassemble control head to mid-plate by reversing the order of Section 5.7.8.

CAUTION: Carefully mate the OBS pot gear (item 81) to the drive shaft gear to keep the OBS pot and azimuth card in alignment.

5.7.9 OBS Pot Replacement

Refer to Figure 6-3

(a) Unsolder the 4 leads from the back of the OBS pot.
(b) Remove the three mounting screws (item 39) that secure the pot to the mid-plate assembly.
(c) Pull the OBS pot and pot gear (item 81) toward the rear of the unit to clear the mid-plate assembly.
(d) Remove the pot gear (item 81) and install on the new OBS pot.
(e) Remount new OBS pot to the mid-plate assembly making sure the pot gear (item 81) is meshing with the pot driver gear.
(f) Solder the 4 leads to the back of the OBS pot.
(g) Realign the OBS pot to the azimuth card per Section 5.8.

5.7.10 DME L.E.D Display Assembly Removal

Refer to Figure 6-3

The L.E.D display assembly is bracket mounted to the front and rear castings by two screws.

(a) Turn the IDME 891 on its side for access to the L.E.D display mounting bracket.
(b) Pry the two ribbon cable connectors from their respective connector pins that are mounted on the display printed circuit board (item 79).
(c) Remove the two #4 flat head screws that secure the display assembly bracket to the front and rear castings.
(d) Gently force the display assembly toward the rear of the unit so the four L.E.D's clear the front casting and then pull the assembly stright down and out.

5.8 OBS POT AND AZIMUTH CARD ALIGNMENT

Refer to Figures 6-3 and 5-2.

In order to electrically zero set the VOR converter, the OBS pot and the OBS azimuth card must be aligned to each other. Alignment is necessary when the OBS pot is replaced and also when the meter or OBS drive shaft is replaced.

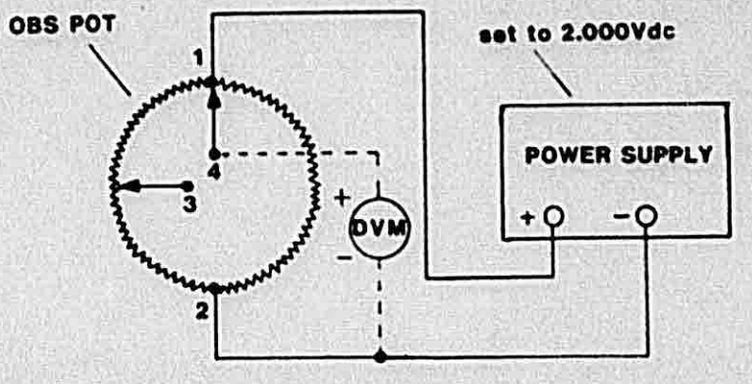


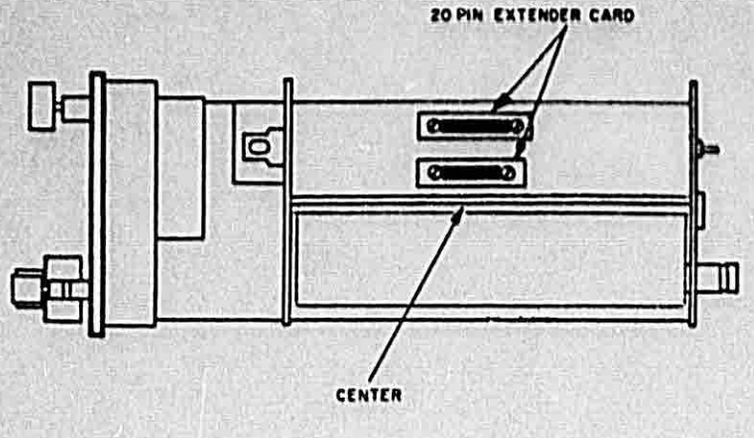
FIGURE 5-2 OBS POT/AZIMUTH CARD ALIGNMENT

The following is the procedure for OBS pot/azimuth card alignment:

1. Set the OBS azimuth card to read 80 degrees.
2. Loosen the two set screws in the OBS driver gear (item 61 of Figure 6-3) so that the OBS drive shaft will not turn the azimuth card. The azimuth card is now disengaged from the drive shaft.
3. Connect a power supply across the OBS pot pins 1 and 2 as shown in Figure 5-2. Set the power supply to 2.000 Vdc.
4. Connect a digital VM across OBS pot pins 2 and 4 as shown in Figure 5-2.
5. Rotate the OBS knob until the digital VM reads 2.000 Vdc.
6. Remove the digital VM's negative lead from OBS pot pin 2 and connect it to OBS pot pin 3.
7. Rotate the OBS knob in a CLOCKWISE direction until the digital VM reads a perfect null (0.000 Vdc).
8. With the OBS azimuth card set at 80 degrees and the OBS pot set at the null point found in step 7; the two are now in alignment. Carefully tighten the two set screws in the OBS drive gear to secure the gear to the shaft.

5.9 EXTENDER CARD TROUBLESHOOTING AID

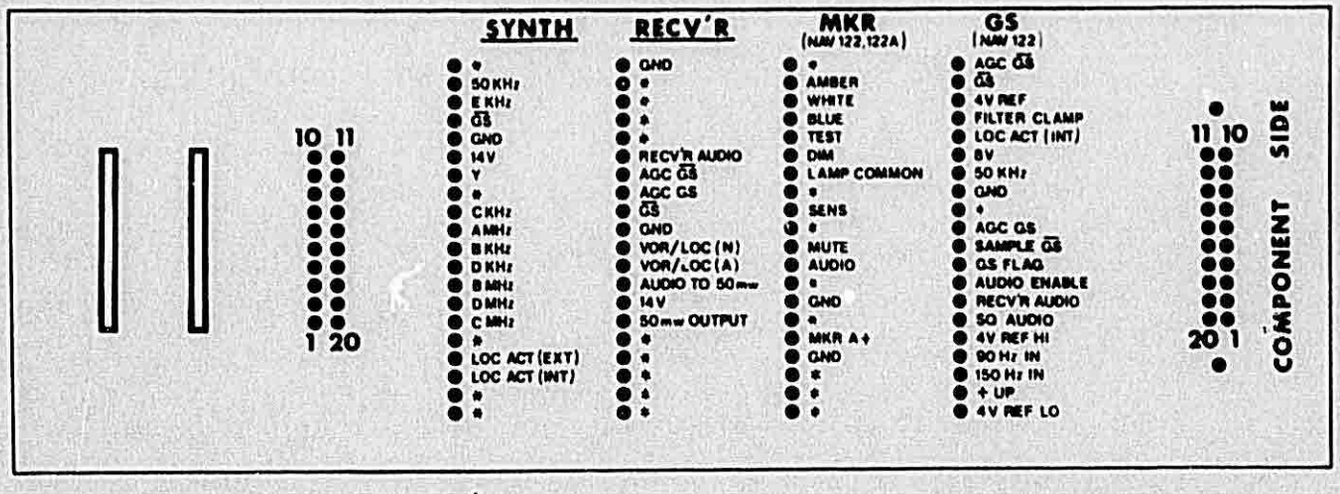
In order to gain access to the IF Receiver/Power Supply board for troubleshooting purposes, a 20 pin card extender must be used (see Figure 5-3). The 20 pin extender card that may be used is the one designed to facilitate the troubleshooting of the NAV 122/121 VOR/ILS radios. There were two extender cards designed for the NAV 122/121 radios; a 20 pin and 26 pin version. The 20 pin version can be used on the IDME 891 to extend either the VCO/SYNTH Board or the IF RCVR/Pwr Supply board. Figure 5-3 illustrates how to use the extender card.

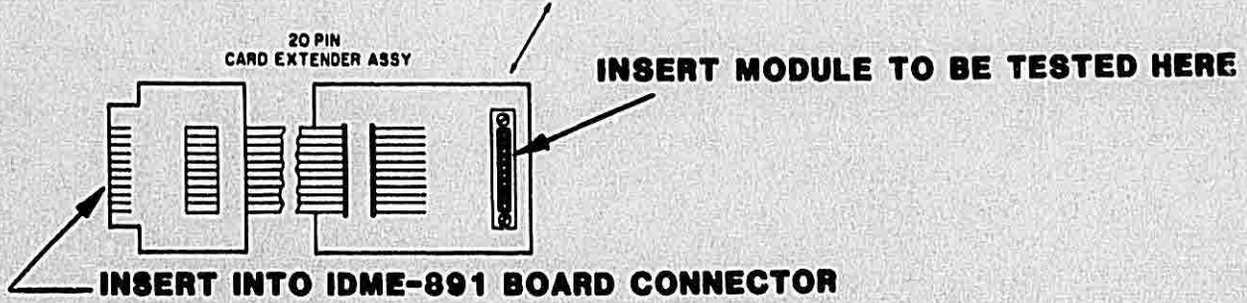


"THIS SIDE OUT" SHOULD ALWAYS FACE AWAY FROM THE CENTER

WARNING!

MISORIENTATION OF AN EXTENDER CARD COULD RESULT IN DAMAGE TO THE MODULE UNDER TEST.





NOTE: TO ORDER THIS EXTENDER CARD, USE PART NUMBER 56163-2111

FIGURE 5-3 20 PIN EXTENDER CARD

5.10 TROUBLESHOOTING FLOWCHART

The troubleshooting procedures are initially given in flowchart Figure 5-4 and further supported by written discussions which include troubleshooting hints.

The IDME TROUBLESHOOTING Flow Chart (Figure 5-4) should be used first as this will provide the troubleshooter with the first level of fault isolation and indicate which additional section to consult.

The flow of the chart leads the user down the page as each question is answered YES. A reply of NO directs the user to the right. If all questions are answered "YES", the DME or circuit in question is operating properly. If any question is answered "NO", the DME is not operating properly and the "NO" line identifies what circuit or component is at fault.

5.11 REPLACEMENT MODULES

Problems isolated to the Power Supply, 63 MHz IF Receiver, VCO/Synthesizer, or Transmitter/Exciter sections of the IDME-891 may be quickly solved by replacing the defective circuit with an exchange module.

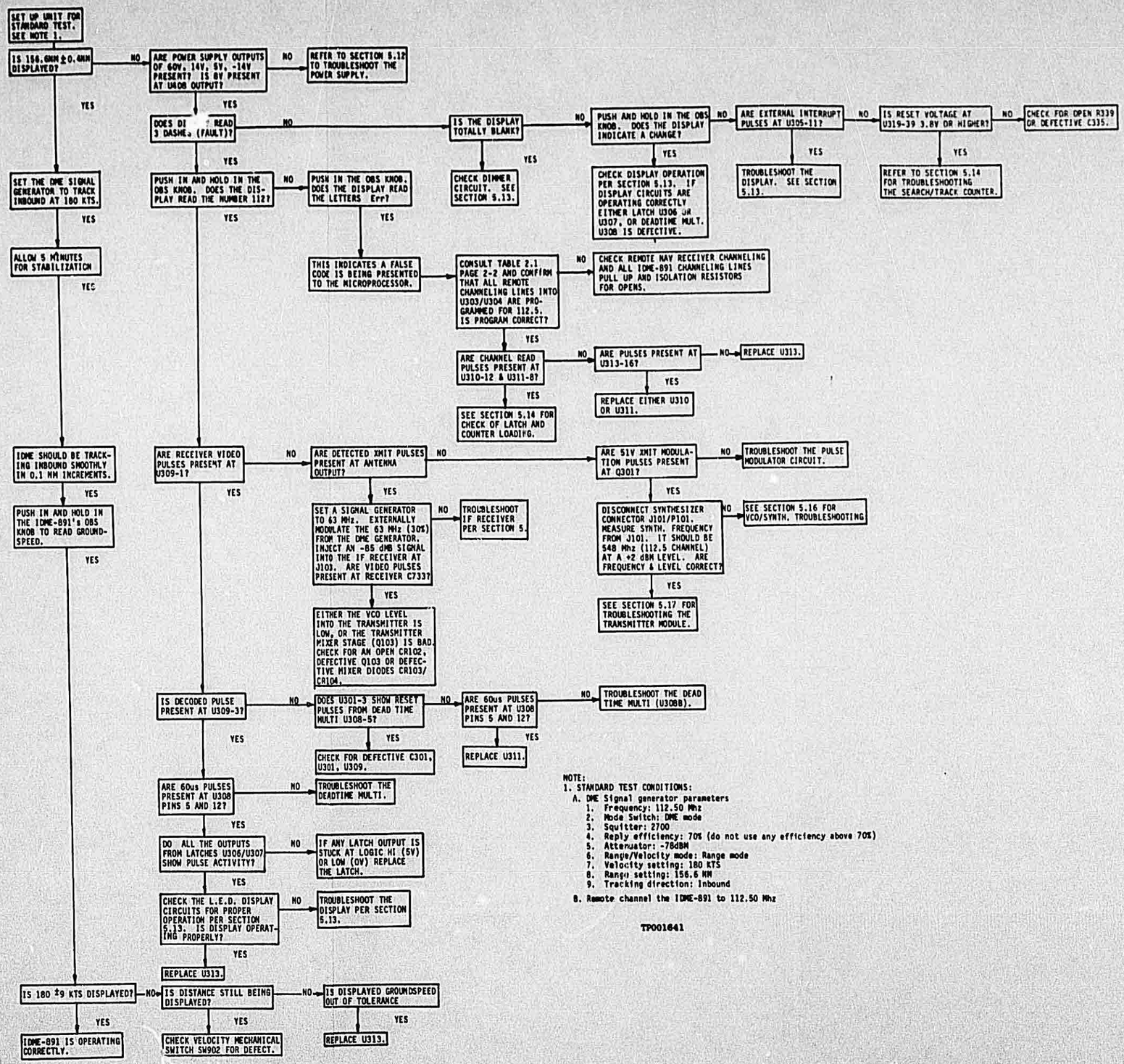
Narco has added three IDME-891 replacement modules to its "module exchange" program. Just order the replacement module, and return the defective module, along with the invoice received with the replacement, to Narco.

Replacement modules may be ordered by using their complete and tested replacement module part number.

MODULE	ORDER NUMBER
VCO/Synthesizer Board	01426-1390
Transmitter/Exciter Assembly	01423-1390
IF Receiver* and Power Supply Board	01427-1390

*IF Receiver not available separately

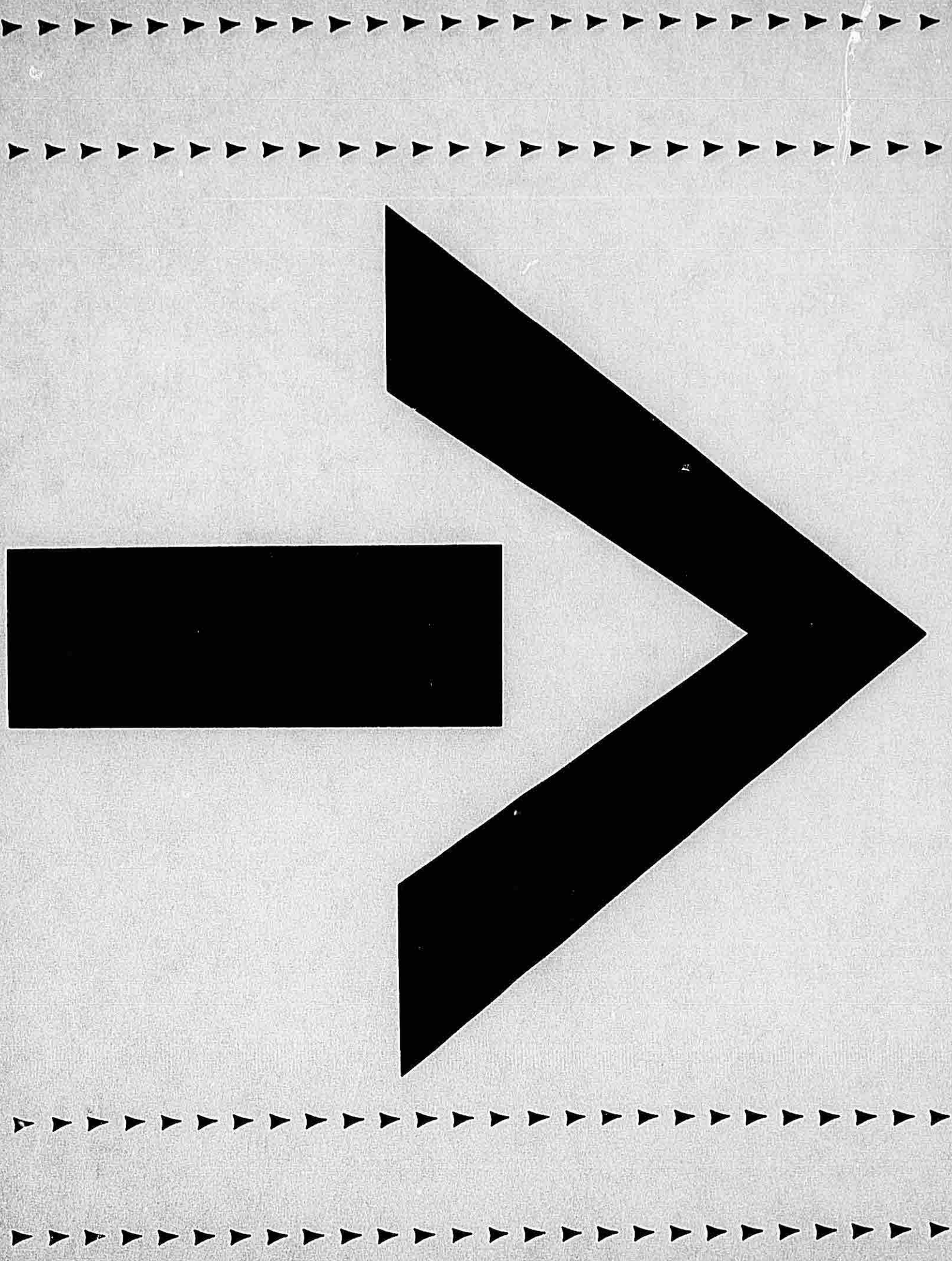
NOTE: The Range and Bottom Interconnect Boards are NOT available on an exchange basis.



NOTE:
1. STANDARD TEST CONDITIONS:
   A. DME Signal generator parameters
      1. Frequency: 112.50 Mhz
      2. Mode Switch: DME mode
      3. Squitter: 2700
      4. Reply efficiency: 70% (do not use any efficiency above 70%)
      5. Attenuator: -78dBM
      6. Range/Velocity mode: Range mode
      7. Velocity setting: 180 KTS
      8. Range setting: 156.6 NM
      9. Tracking direction: Inbound
   B. Remote channel the IDME-891 to 112.50 Mhz

TP001641

FIGURE 5-4 DME TROUBLESHOOTING FLOW CHART

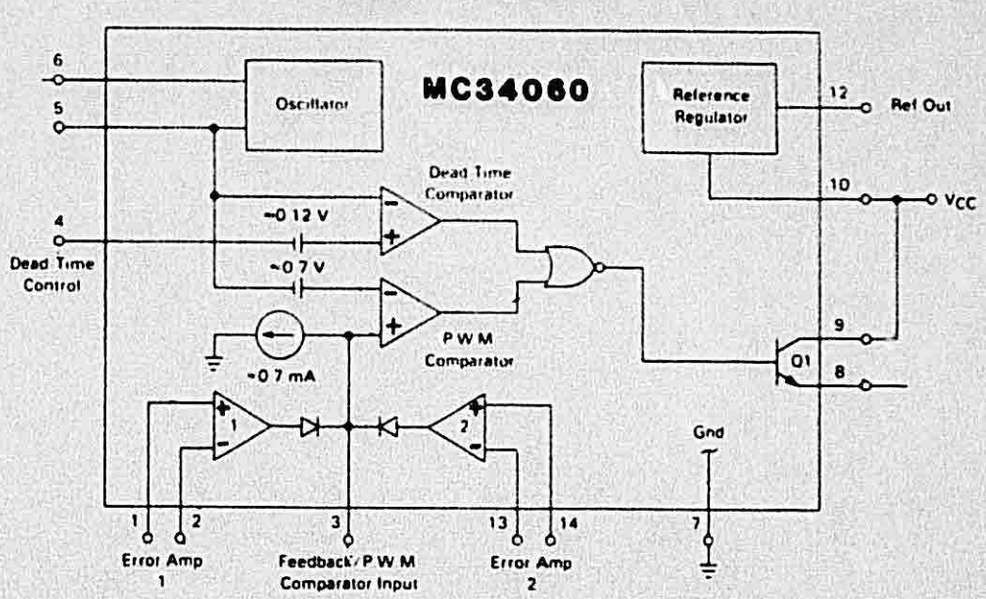


5.12 POWER SUPPLY TROUBLESHOOTING

> NOTE: The complete Power Supply/IF Receiver module is available on an exchange basis. Section 5.11.

Shown here is a block diagram of U801, the Motorola MC34060 Pulse Controller IC. Use this block diagram and the power supply schematic figure 6-7 found on page 6-16 to troubleshoot any power supply problems.

U801 BLOCK DIAGRAM



If the power supply voltage outputs do not meet the following tolerances, then troubleshooting is required:

VOLTAGE OUTPUT	SPECIFICATION
+60 Vdc	63V max, 57V min
+14 Vdc	14.7V max, 13.3V min
+ 5 Vdc	5.3V max, 4.7V min
-14 Vdc	-14.7V max, -13.3V min

In order to gain access to the power supply module for troubleshooting purposes, the extender card (see section 5.9) may be used. However, it is preferred to troubleshoot the power supply module without using the extender card by completely removing the module from the IDME-891. When choosing this latter method, the following preparations must be made prior to troubleshooting the module:

1. Connect a 14 Vdc power supply (initially turned off) across CR-801 to furnish power to the module.

5.12 POWER SUPPLY TROUBLESHOOTING, continued

2. Load the outputs of transformer T801 as follows:

   a. Solder a 100K resistor from the cathode of CR802 to ground
   b. Solder a 6.8K resistor from the cathode of CR803 to ground
   c. Solder a 150 ohm resistor from the cathode of CR804 to ground
   d. Solder a 6.8K resistor from the cathode of CR805 to ground

3. Unsolder the 14V input to the IF receiver at E801/C734 (See component layout)

5.12.1 Power Supply Module Troubleshooting Procedure

The procedures given here require that the power supply module be completely removed from the IDME-891 and properly loaded with resistors as outlined in Section 5.12.

A power supply problem may be the result of a defect in the module itself. However, a problem on either the VCO/Synthesizer module, exciter/transmitter module, range board or bottom interconnect board could load down the power supply and prevent it from operating properly. The first three procedural steps will prove if the fault exists in the power supply module.

1. Check for a blown fuse F801 and replace if necessary.
2. Check the emitter/base, emitter/collector and base/collector of Q801 for opens or shorts. Replace if necessary.
3. With F801 and Q801 known to be good, connect a bench power supply (preset to 14 Vdc and turned off) across CR801:
   a. Turn on the bench power supply and observe its ammeter. The normal current draw should be 62 milliamps.
   b. If the current draw is serval amps, turn off the bench power supply and check for a shorted filter capacitor (C805, 806, 807,808), a shorted rectifier diode (CR802, 803, 804, 805), or a defective T801.
   c. If the current draw appears normal, check all output voltages for rated values.

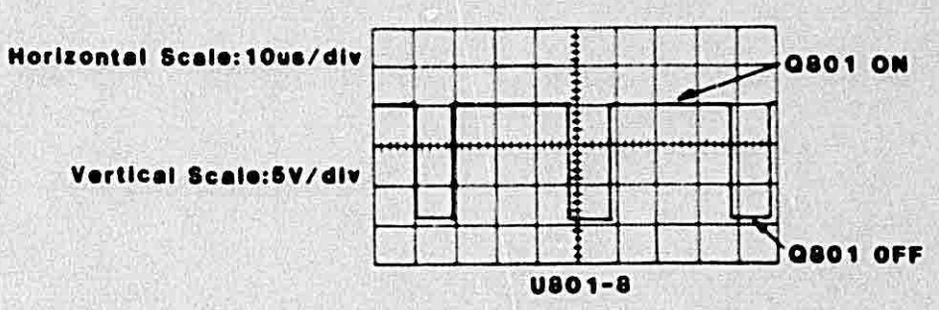
      If voltages meet specifications, resolder the 14V IF receiver power lead at E801/C734 and check that lead for rated value.

If all voltages are correct, then the power supply module is working properly and a problem must exist on some other module. TO GO STEP 11.

      If rated values are NOT correct, then the power supply module is defective. Continue on to Step 4.
4. Turn off the bench power supply and jumper the base of Q801 to ground. Do not remove jumper until instructed to do so.

5.12.1 Continued

5. Turn on the bench power supply and measure the internal reference regulator of U801 at pin 12. It should read 5.0 ±0.3 Vdc. If out of tolerance, replace U801. This same reference voltage should also be at U801 pin 2.
6. Check the internal oscillator of U801 at pin 5 with an oscilloscope. It should appear as the upper trace in waveform #1 photograph shown on page 6-17. The sawtooth waveform frequency should be between 18 to 25 Khz. If the frequency is out of tolerance or the waveform is missing or abnormal, first check C804 and R807 for cold solder joints and proper values before replacing U801.
7. Check the deadtime bias at U801 pin 4. It should be 0.5 Vdc ±0.2V. If the bias is missing, check for an open R803. If the bias at pin 4 measures 5V, check for a shorted C803 or open R806.
8. Monitor U801 pin 8 with an oscilloscope. The output pulses should have a voltage level and duty cycle as shown here.



Because the base of Q801 is shorted (Step 4), the 5 volt feedback line from CR804 into pin 1 of U801 via R804/R805) will be at zero volts. The response from U801 will be to drive Q801 ON as hard as possible.

The waveform picture indicates the maximum drive possible into the base of Q801 (10us OFF and 30usec ON).

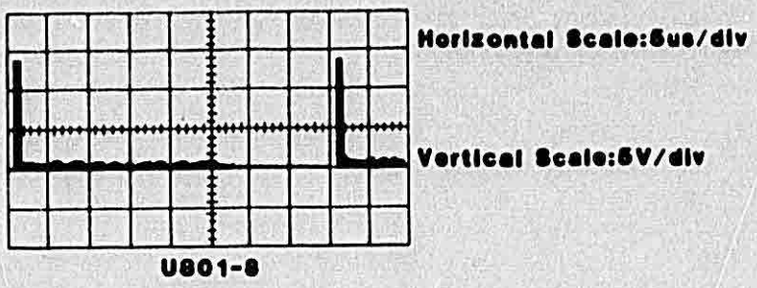
If the pulses are missing or the ON time is considerably less than 30usec, replace U801.

9. If the output pulses from U801 pin 8 are proper, then the three following tests should each cause the output from U801 pin 8 to drop to zero volts during the test.
   a. Briefly short U801 pin 4 to pin 12
   b. Briefly short U801 pin 3 to pin 12
   c. Briefly short U801 pin 1 to pin 9

   Failure of any test to produce zero volts at pin 8 would indicate a defective U801. If all three tests are successful, then U801 is operating properly.

5.12.1 Continued

10. Remove the jumper from the base of Q801 and check for the following conditions:
    a. 14V pulses of 0.5usec width at a frequency of 18 to 25 Khz shall be present at U801 pin 8 as shown here.



U801-8

    b. The collector waveform shall be as shown in photograph #2 on page 6-16.
    c. All voltage outputs from T801 shall be at their rated values. Failure to obtain rated output voltages or proper waveforms would indicate either an open rectifier diode or an open filter capacitor. If diodes and capacitors check out properly, then T801 is defective.
11. If all output voltages are at rated values then the power supply module is operating properly. Remove all load resistors and install the module in the IDME-891.
12. Isolate the problem to a specific circuit board or module as follows:
    a. Remove the VCO/Synthesizer module from the IDME-891. If all output voltages from T801 are correct then troubleshoot the VCO/Synth module. If outputs are not correct, then reinstall VCO/Synth module.
    b. On the Exciter/Transmitter module, unsolder the -14V lead from feed-thru FL104, and the +14V lead from FL101. If all output voltages are correct, troubleshoot the Exciter/Transmitter module.
    c. If output voltages are not correct, then troubleshoot the range and bottom interconnect boards.

5.13 DISPLAY CIRCUIT TROUBLESHOOTING

SERVICE NOTE: Proper operation of the display is NOT POSSIBLE unless the counter chain (U303, U304 and U305) is able to complete its count of 2048 clock pulses and issue an external interrupt pulse (U305-11) to the microprocessor. Microprocessor operation is dependent upon the steady receipt of external interrupt pulses (U305-11). What may appear to be a display problem could be a counter defect. Therefore, confirm the existence of external interrupt pulses to determine where the troubleshooting effort should be applied, display or counter circuitry.

5.13 DISPLAY CIRCUIT TROUBLESHOOTING, Continued

The display consists of four L.E.D's mounted on a removable bracket. If access or removal is required, consult Section 5.7.10 on page 5-10.

Refer to the schematics on pages 6-25 and 6-27 when troubleshooting the display circuitry.

The following troubleshooting procedures are based on the assumption that external interrupt pulses are present at U305-11 as shown in the upper trace of waveform photograph #24 on page 6-24:

1. Execute the following proof of performance test:
   a. Channel the IDME-891 to 108.00 Mhz and remove the RF signal from the DME signal generator.
   b. The display should indicate 3 dashes ("g" segments) with the decimal point illuminated.
   c. Push the IDME-891's OBS Knob in and hold in. The display should read the number 108.
      Note: If the display reads the letters "Err", this indicates a false channel code is being presented to the microprocessor. A problem must exist at the remote channeling source or with the IDME-891's data latches, input channeling lines or failure of a counter to load properly.
   d. Short to ground pin 10 (lamp test) of either U502, U504 or U506. The display should read the number 188.8. Release the short from pin 10.
   e. Rotate the IDME-891's dimmer control knob to confirm dimming action.
   f. Restore RF signal to unit and check the display for proper readout for the following ranges: 0.8, 1.8, 88.8 and 158.6 NM.

   If all tests are met, then the display circuitry is operating properly. If the display fails the test, then proceed to Step 2.
2. Confirm the presence of decoder enable pulses at U314-5 as shown in waveform photograph #24 on pages 6-24. Absence of pulses would indicate a microprocessor failure or pin 5 of U314 is internally shorted.
3. Confirm the presence of multiplexing pulses A0, A1, A2 at pins 1, 2 and 3 of U314. Refer to waveform photograph #27 on page 6-24. Absence of any pulses would indicate a microprocessor failure or an internal short in U314.
4. Confirm the presence of latch clock pulses at pins 2, 3, 5, 6, 10 and 11 of U315. See waveform photograph #28 on page 6-24. Absence of any pulses would indicate a failure of U314.

5.13 DISPLAY CIRCUIT TROUBLESHOOTING, Continued

5. Confirm the presence of latch pulses at pins 4, 7 and 9 of U315. Absence of any pulse indicates a failure of U315.
   a. Push in and hold in the OBS Knob and confirm that pulses are still present at pins 4, 7 and 9. If pulses are absent, monitor U315-1 with a voltmeter. It should read zero volts when the OBS Knob is pushed in because switch SW-902 (actuated by OBS Knob) should ground this pin. If switch is working, then replace U315.
6. Confirm the presence of pulses at dimmer timer U507-3. Refer to waveform photograph #30 on page 6-27. If pulses are present, then rotation of the display dimmer knob should change the duty cycle of the pulses. If pulses are absent troubleshoot the dimmer circuit.

> SERVICE NOTE: U507-3 is simultaneously applied to the dimmer control inputs (pin 1) of latches U501, U503 and U505. When pin 1 is logic high (5V), then all the Q outputs of the latches go to a high impedance state, shutting off all drive to segment drivers U502, U504 and U506. It is the ratio between the time U507-3 is high (latches Off) versus the time it is low (latches on) that creates dimming action.
>
> If U507-3 is stuck high (5V), then the display will be totally blank. If it is stuck low, there will be no dimming action and the display will be uniformly bright.

7. Confirm the presence of pulses at ALL segment and decimal point outputs of the microprocessor (pins 26 thru 33). If any segment output shows a constant logic low (0V) state, short pin 39 (reset) of the microprocessor to ground. In the reset state, all segment output lines must go to the logic high (5V) state. Failure of any output to go high indicates a defective microprocessor.
8. Confirm the operation of latches U501, U503, U505 and segment drivers U502, U504, U506 by observing pulse activity at all outputs. An inactive output indicates a defective device.

   If a doubt exists as to whether a latch/segment driver combination is working properly, then perform the following test to confirm operation:
   a. Turn off the IDME-891 and jumper the microprocessor reset line (pin 39) to ground.
   b. Turn on the radio. The latch clock lines at U315 pins 4, 7 and 9 will all be logic high (5V) as will be all segment lines.
   c. Briefly short U315-4 to ground and observe the first two digits in the display. They should read the numbers 1 and 8 which would confirm the operation of U501 and U502.

5.13 DISPLAY CIRCUIT TROUBLESHOOTING, Continued

d. Briefly short U315-7 to ground and observe that digit #3 reads the number 8 and the decimal point is illuminated. This confirms operation of U503 and U504.
e. Briefly short U315-9 to ground and observe that digit #4 reads the number 8. This confirms the operation of U505 and U506.

Failure of any one of the 7 segments to illuminate would indicate either a latch or driver failure.

5.14 SEARCH TRACK COUNTER AND DATA LATCH TROUBLESHOOTING

The counters (U303, U304, U305).will count 2048 clock pulses, and the 2048th pulse is extracted from U305-11. This pulse is identified as the "External Interrupt" pulse and is coupled into pin 38 of the microprocessor. The microprocessor depends upon a steady receipt of these pulses for its operation, for without them, the microprocessor is INOPERATIVE.

The 74HC161 counters operate in either of two modes; counter or load.

When operating in the count mode the reset (pin 1), CET (pin 10), CEP (pin 7) and PE (pin 9) inputs MUST all be logic high (5V).

When operating in the load mode, the reset (pin 1) MUST be logic high and the PE (pin 9) MUST be logic low. The logic level of the other inputs are not relevant.

The load mode is used to extract the logic level of the remote channeling lines which indicate what frequency has been selected. This information is latched into the microprocessor to program the VCO/Synthesizer. The channel read pulses (U313-16) activate the load mode.

The following procedures may be used to troubleshoot or confirm proper operation of the search track counter:

5.14.1 Counter Mode Troubleshooting

NOTE: Prior to any troubleshooting, push and hold in the IDME-891's OBS Knob and observe the L.E.D. display. If the display reads the letters "Err", check U311B for a failure, or other remote channeling lines for a false code condition. When a false code exists, the microprocessor will drive the search enable output (U313-5) logic low which shuts down the search track counters.

1. Confirm presence of system clock pulses at U310-8 as shown in waveform photograph #20 on page 6-24.
2. Confirm presence of counter clock pulses at U302-9 as shown in waveform photograph #20 on page 6-24. If clock is missing, replace U302.

5.14.1 Counter Mode Troubleshooting, Continued

3. Confirm presence of external interrupt pulses at U305-11 as shown in waveform photograph #24 on page 6-24. If pulses are present the counter chain is operating properly. Go to Section 5.14.2 to check the load mode operation.

   If the pulses are missing at U305-11 continued on to Step 4.

4. If pulses are missing at U305-11, then check for presence of pulses at U303-15 and U304-15 as shown in waveform photograph #23 on page 6-24.
   a. If pulses are present at U304-15, then replace U305.
   b. If pulses are missing at U304-15 but present at U303-15 then replace U304.
   c. If pulses are missing at U305-15 go to Step 5.
5. If the pulses are missing at U303-15 then use an oscilloscope to check the following microprocessor outputs:
   a. The data clear line U313-4 must be logic high (5V)
   b. The search enable line U313-5 must be logic high (5V)
   c. The channel read line U313-16 must be logic low (0V) and this line inverted to logic high (5V) by U310-12.

   If all these conditions are met, then U303 should show TC pulses at its pin 15; if not, replace U303.

   If all the above conditions are not met, the search track counter will remain inoperative.

   If either or both U313-4 and U313-5 are stuck low, then cut the pins at the microprocessor to isolate these outputs from the printed circuit tracks. Jumper the isolated printed circuit tracks to a 5 volt source such as pin 16 on U306 or U307.

   If U313-16 were stuck logic high (5V), this would permanently set the counters to the load mode. Jumper U313-16 to ground if it is stuck at 5 volts.

   When all conditions are satisfied, check U303-15 for output pulses, and if missing replace U303. If pulses are present at U303-15, then the microprocessor is defective.

5.14.2 Load Mode Troubleshooting

A pair of positive channel read pulses from U313-16, which are inverted by U310E, are used to place the counters in the load mode. Remember, the counter chain must be operational in order to supply the microprocessor with external interrupt pulses or else the microprocessor cannot generate the channel read pulse pair.

Check for proper operation as follows:

1. Confirm the presence of the channel read pulse pair at U310-12 and U310-13 as shown in waveform photograph #18 on page 6-24.

   If missing at U310-13 replace U313. If missing at U310-12 replace U310.

5.14.2 Load Mode Troubleshooting, Continued

2. If the channel read pulse pair are present at U310-12, then jumper U310-12 to ground. This places all the counters in the load mode. Channel the remote NAV receiver (or channeling source) thru all the Mhz and Khz frequencies and check that each "Q" output from U303/U304 and the Qo output from U305 will transition between 0 and 5 volts.

   If any "Q" output fails to make a transition, replace that integrated circuit.

5.14.3 Data Latch Troubleshooting

Data Latches U306/U307 transfer the logic state of their "D" inputs to their "Q" outputs upon the receipt of a clock pulse which can be either the channel read pulse pair from U313-16 or a decoded reply pulse from U309-3.

The following procedure assumes that the search track counters and microprocessor are operating properly.

1. Confirm the presence of the channel read pulse pair at U311-8. If missing replace U311.
2. Confirm the presence of a decoded reply pulse at U309-11. If missing replace U309.
3. Check for proper data latch operation as follows:
   a. Remove or disable the remote NAV receiver's channeling lines. This will force all the IDME-891's remote channeling lines to their logic high (5V) state.
   b. All of the "D" inputs to U306/U307, except D4 of U307, should be logic high (5V). The inputs should be transferred to the "Q" outputs by the channel read pulse pair. Any "Q" output, other than Q4 of U307, which should be logic low, that measures logic low (0V) would indicate a defective latch.
   c. If all data latch outputs are at their correct logic level, short U313-4 to ground and check all the data latch outputs for a logic low state. Any output that remains logic high would indicate a defective latch.

5.15 63 Mhz IF RECEIVER TROUBLESHOOTING

NOTE: The IF Receiver is attached to a printed circuit board module that also contains the power supply circuitry. A replacement module, consisting of both the IF receiver and power supply, is available on an exchange basis. The order number is 01427-1390. The IF receiver assembly, by itself, is NOT available on an exchange basis.

To gain access to the IF receiver for troubleshooting purposes, the extender card (see page 5-12) may be used. However, it is possible to successfully troubleshoot the IF receiver with the IF receiver/power supply module completely removed from the radio.

5.15 63 Mhz IF RECEIVER TROUBLESHOOTING, Continued

The following service procedures are based on this latter method.

1. Disconnect the RF cable at P103/J103 and completely remove the IF receiver/power supply module from the radio.

   Remove the shield from the IF receiver assembly to expose the circuitry.
2. Set the bench power supply to 14 Vdc and connect the negative power lead to the anode of CR801 and the positive lead to the cathode of CR803.
3. Measure all DC voltages at the points indicated in Figure 6-8, the IF Receiver Schematic, on page 6-17. All voltages have a tolerance of ±10% except the base bias voltages of transistors Q706 to Q710 which have a ±5% tolerance. Any base voltage of these transistors that differs by 60 millivolts from the others in this group may be suspected of having poor gain.
4. Set a VHF signal generator to 63 Mhz and externally modulate (30%) the generator with the DME signal generator.
5. Connect a resistance substitution box set to 10K ohms between C733 and C732.
6. Monitor C733 with an oscilloscope.
7. Inject the 63 Mhz pulse modulated signal into J103. A signal level of -87 dBM shall produce a video pulse pair at C733. At this threshold signal level the video pulse pair will show considerable noise. As the signal level is increased and AGC action takes hold, the noise will decrease and the video pulse pair will show a firm appearance.
8. If the video pulse pair is present with a -88 dBM signal level, the gain of the IF receiver is normal and proper AGC action should be checked by monitoring the collector of Q701 with a digital voltmeter. At a signal level of -88 dBM the AGC voltage is approximately 7 volts. At -77 dBM it is 6 volts and at -67 dBM it is 4.5 volts.

   If the IF receiver meets the above conditions it may be assumed to be operating correctly.
9. If the video pulse pair is not present at C733 with a -88 dBM signal level, increase the signal level to -77 dBM. If the pulses are still not present, monitor the anode of the detector diode CR701 with an oscilloscope. If the pulses are present (see waveform photograph #4 on page 6-17) then troubleshoot from this point forward.

   If the pulses are missing at CR701, then it may be assumed the problem is in one of the filter stages from Q710 to Q706.
10. To isolate the problem to a particular filter stage, the following 63 Mhz RF signal injection levels are given for the three coupling capacitors C723, C717 and C710. When injecting the RF signal, remove one lead of the capacitor from the printed circuit board at the tuning coil side (L704, L706, L708) and inject the signal into this lead. Keep the resistance substitution box (10K) between C732 and C733. Monitor C733 with the

5.15 63 Mhz IF RECEIVER TROUBLESHOOTING, Continued

oscilloscope to confirm the presence of the video pulse pair for each injection point.

INJECTION POINT	RF SIGNAL LEVEL	MONITOR C733
Connector J103	-87 dBM	Video pulse pair
C723	-64 dBM	Video pulse pair
C717	-54 dBM	Video pulse pair
C710	-44 dBM	Video pulse pair

5.16 VCO/SYNTHESIZER TROUBLESHOOTING

NOTE: The VCO/Synthesizer module is available on an exchange basis. The order number for a tested replacement module is 01426-1390.

Table 4.1 on page 4-3 lists the VCO output frequency, as measured from J101, for every channel from 118.00 to 117.95 Mhz. The power output from J101 should be +2 dBM ±0.5 dBM. Confirmation of proper operation is made by connecting a frequency counter and RF wattmeter to J101 to verify correct frequency and power.

The following procedures are given as a troubleshooting guide for the VCO synthesizer:

1. Verify that all DC voltages are present:
   a. +14 V at the input to U408 (3 terminal regulator)
   b. + 8 V at output of U408
   c. -14 V at R415
   d. + 5 V at U404-10
2. Verify that 250 Khz reference pulses are present at U407-14 as shown in waveform photograph #10 on page 6-19.
3. Perform a VCO voltage tuning check as follows:
   a. Connect a digital voltmeter to FL402
   b. Remote channel the IDME-891 to 108.00 Mhz. The VCO voltage should be 1 Vdc (low limit: 0.6V, high limit: 1.3V)
   c. Remote channel the IDME-891 to 117.90 Mhz. The VCO voltage should be 7 Vdc (low limit: 5.8V, high limit: 7.3V)

   Note: Each Mhz channeling step changes the VCO voltage in approximately 0.5V increments. Each Khz channeling step yields approximately 0.05V increments.

   If the VCO voltage tracks but appears to be out of tolerance, retune as outlined in Section 5.5.2, page 5-4.

   If the VCO voltage does not track and is stuck at a constant voltage, continue on to Step 4.

5.16 VCO/SYNTHESIZER TROUBLESHOOTING, Continued

4. Check for proper programming of code converter U402 as follows:
   a. Remote channel the IDME-891 to 108.00 and 117.90 and consult the "ARINC TO SYNTHESIZER" code conversion table found on page 6-19 and check all "Q" outputs of U402 for proper logic levels. (X=logic Hi=5V, 0=logic low=0V)

   If U402 programming is not correct, push in the IDME-891's OBS knob and ensure that the display does not read "Err" as this would indicate that a false ARINC code is being presented to the microprocessor. If "Err" is not displayed then U402 may be considered defective. The chance that the microprocessor is sending the wrong data to U402 is possible but unlikely.
5. If the programming of U402 is correct, then check the VCO oscillator (Q401) and VCO buffer (Q402) for operation as follows:
   a. Connect a frequency counter to J101
   b. Unsolder the VCO tuning lead from FL402. Connect a separate power supply to FL402 to simulate the VCO tuning voltage. Vary the power supply voltage between 1 and 7 volts and observe if the frequency counter will track frequencies from 520 to 575 Mhz.
   c. If the frequency counter indicates only partial tracking or indicates NO output from J101 then troubleshoot the VCO oscillator and VCO buffer circuits.
6. If the frequency counter indicates that the VCO circuits are tracking the simulated tuning voltage, adjust the power supply voltage to give a 570 Mhz output at J101 and let it sit at this frequency.
7. Check U401-11 for clock pulses as shown in waveform photograph #8 on page 6-19 (check clock at U404-2).

   If pulses are missing, then check U401-15 with a frequency counter. The frequency should be 1/2 (285 Mhz) of that measured at J101. If the frequency is present at U401-15 and at an 0 dBM level, then U401 is defective.

   If the frequency at U401-15 is missing or incorrect, trouble-shoot the ÷2 prescaler circuit.
8. If pulses are present at U404-2, remote channel the IDME-891 to 117.90 Mhz. Check for output pulses at U407-3 as shown in waveform photograph #10. If present, go to Step 11.

   If pulses are missing, check the logic level of U406-11. If it is logic low, replace U406. If U406-11 is logic low, all counters will be stuck in the load only mode.
9. If U406-11 is logic high (5V), check for output pulses from U405-15. If pulses are present replace U406. If not present, replace U405.

5.16 VCO/SYNTHESIZER TROUBLESHOOTING, Continued

10. If pulses are present at U405-15, then check the ÷10/11 mode counter (U403/U404) as follows:
    a. Remote channel the IDME to 117.90 Mhz. This will set all Khz lines (B1,B2,B4,B8) from U402 to the logic low state.
    b. Short U404-9 to ground. Both pins 11 and 13 of U404 shall measure logic low (.0V). If not, replace U404. Keep the short at U404-9.
    c. When U404-11 and U404-13 are low, U403-3 shall be logic high (5V). If not, replace U403.
    d. If U403-3 is logic high, release the short from U404-9. There should be pulses present at pins 1 and 2 of U403. If not, replace U404.
    e. If pulses are present at U403-1 and U403-2, then U403-3 should have pulses present. If not, replace U403.

    If pulses are present at U403-3 then the ÷N counter circuits are all operating correctly.

11. Check the phase locked loop (U407) for correct operation as follows:
    a. Remote channel the IDME to 110.9 Mhz.
    b. Connect the frequency counter to J101.
    c. Connect a digital voltmeter to U407-13.
    d. Adjust the power supply that is simulating the VCO tuning voltage such that the frequency counter reads 537 Mhz. The voltage at U407-13 should read approximately 7.8 Vdc.
    e. Readjust the frequency to read 533 Mhz. The voltage at U407-13 should read 0 Vdc.

    If the response from U407-13 is not as indicated above, replace U407.

12. The loop filter (C423,C424,R422,R423) may be suspected of not filtering properly if the frequency at J101, as measured on a frequency counter, exhibits an instability in the 100Khz digit.
    (535.000 MHZ)
    └──100 Khz digit

5.17 EXCITER/TRANSMITTER TROUBLESHOOTING

NOTE: The exciter/transmitter module is available on an exchange basis. To order a complete and tested replacement module, use part number 01423-1390.

The exciter/transmitter assembly is aligned at Narco with a spectrum analyzer and a pulse-sweep generator. Without this type of equipment, the transmitter section cannot be aligned. Therefore, Q101 (frequency doubler) and Q102 (power amplifier) are NOT field replaceable. All other transistors may be replaced in the field.

5.17 EXCITER/TRANSMITTER TROUBLESHOOTING, Continued

The following procedures are given as a troubleshooting guide. It is assumed that the transmitter has no detected output pulse pair, or is weak across the band, or exhibits a power reduction at either or both ends of the band.

1. Confirm the presence of the 51V modulation pulse pair at FL102. If missing, check modulator circuit on the range board.
2. Confirm the presence of the modulation pulses at the test points as indicated in waveform photographs 11 and 13 found on page 6-21.
3. Disconnect the VCO connector J101/P101. Measure the DC bias voltages in the exciter stages as indicated in the schematic found on page 6-21. Troubleshoot any abnormal stage.
4. Measure the VCO injection power. It should be 2.5 ±0.5 dBM. If any doubt exists about the VCO injection power, substitute a signal generator for the VCO. Consult Table 4.1 on page 4-3 for the VCO frequencies and inject a +3 dBM CW signal into the exciter.
5. Confirm operation of Q205 as follows:
   a. Reconnect P101/J101 and remote channel the IDME to 112.50 Mhz. If a signal generator is being used in place of the VCO/synthesizer, inject a +3 dBM 548 Mhz CW signal into J101.
   b. Using a 27K isolation resistor, connect a VTVM to the base of Q205.
   c. If the exciter stages Q201 to Q204 are working properly, the base voltage will be approximately +0.3 Vdc ±20%.

      NOTE: When no RF signal is applied to the exciter via J101, the base voltage at Q205 is approximately +1.0 Vdc.

      If an exciter stage transistor must be replaced, consult Section 5.5.5.2 for the proper tuning procedure.
6. Confirm operation of the doubler Q101 as follows:
   a. Disconnect P101/J101.
   b. Monitor C110 with an oscilloscope
   c. The sawtooth waveform that should be present at C110 should have a peak amplitude of 700 millivolts or less.
   d. Connect P101/J101. The sawtooth waveform's peak amplitude should rise to 1.5 Volts or greater indicating that it is being turned on by the RF signal from Q205. See waveform photograph #12.

      If Q101 is defective, the exciter/transmitter module must be exchanged as Q101 is not field replaceable.
7. If Q101 is working properly and the output pulse pair from antenna J102 do not meet specifications, then either Q102 or CR101/CR102 is defective. Ensure that the reverse biasing pulse pair is present at CR102. See waveform photograph #13.

   If Q102 is defective, exchange the exciter/transmitter module, as Q102 is not field replaceable.

NARCO AVIONICS IDME-891

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

6.1 GENERAL

This section contains schematics, component location drawings, and Replacement Parts Lists. There are two sections of Replacement Parts, the Mechanical Parts List and the Electrical Parts List.

6.2 MECHANICAL PARTS LIST

The Mechanical Parts List section is intended to locate, identify and show part relationship to the Unit itself. A simplified exploded view drawing of the control head assembly and chassis assembly is provided to show a complete hypothetical mechanical dissembly of the Unit. Each item shown in the artwork is identified by a balloon with an item number or electrical symbol or both.

The PC board assemblies comprising the DME circuitry are shown in the Mechanical Parts List section only to identify, if any, those replaceable mechanical parts on the board.

6.3 SCHEMATICS

A set of schematics and support information for the IDME 891 is provided in this section. Such support information comprises:

- Component location drawings
- Voltage test points
- Waveforms
- Electrical Parts List on the reverse side of the schematic

6.4 ELECTRICAL PARTS LIST

The Electrical Parts List will be found on the reverse side of each schematic. The parts listed are those found in the schematic.

The list contains such data as: the electrical symbol number, Narco Part Number, Description and its component assembly and schematic grid coordinates.

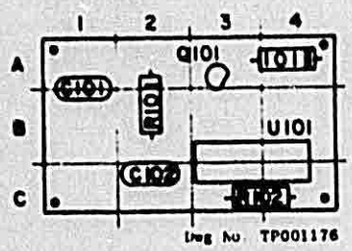
6.4.1 Using the Electrical Parts List

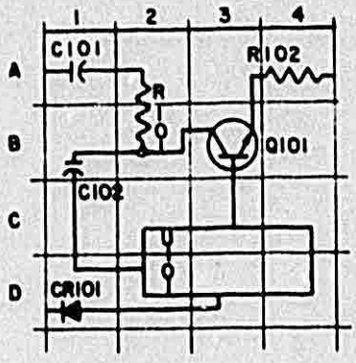
To the far right of the part number/description one will find a grid coordinate listing for that part. One set of coordinates locates the part on the component assembly drawing, the second locates the part within the schematic. Where a part, such as an IC, is comprised of several internal subsections, each subsection is located for the user.

Grid coordinates are shown along the top or bottom and left sides of both the component assembly drawing and schematic. The actual grid lines are not, in themselves, shown to avoid clutter.

6.4.1 Continued

The grid coordinate identifies that grid box wherein the component's symbol letter is located as shown in the sample below:





	Component Grid	Schematic Grid
C101	A1	A1
C102	C2	C1
CR101	A4	D1
Q101	A2	B4
R101	B2	A2
R102	C3	A3
U101	B4	C2

6.5 MODIFICATION LABEL

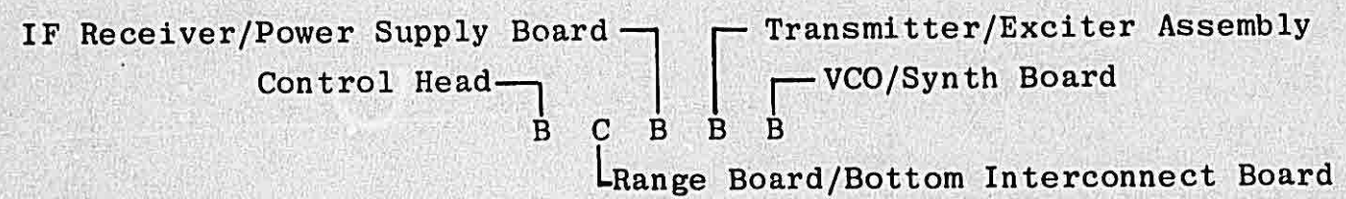
The modification label affixed to the Unit's rear plate is provided to allow quick recognition of what modifications were made to that Unit, if any. Thus, the block should only be filled in upon completion of a Narco Service Bulletin Modification Instruction. Fill in only that block or blocks that the Bulletin designates.

6.6 SERIAL NUMBER V/S CHASSIS LEVEL CONFIGURATION CODE

The 5-digit serial number will be the Key factor to identify units. The serial number is found on the modification label affixed to the unit's rear plate.

The Chassis Level Configuration Codes will be used when necessary to identify specific subassemblies at specific levels. The Unit's Chassis Code is stamped, as a series of letters, in ink on the Unit's rear plate.

Their arrangement and identity are shown here.



6.7 MODULE EXCHANGE PROGRAM

Narco has added three IDME 891 PC modules to its module replacement program. The modules are available on an exchange basis, ready when the need calls. The object of the program is obvious, - to provide fast customer service.

Replacement modules may be ordered by using their complete and tested replacement module part number.

MODULE	ORDER NUMBER
VCO/SYNTHESIZER PC BOARD	01426-1390
IF RECEIVER/POWER SUPPLY PC BOARD	01427-1390
TRANSMITTER/EXCITER ASSEMBLY	01423-1390

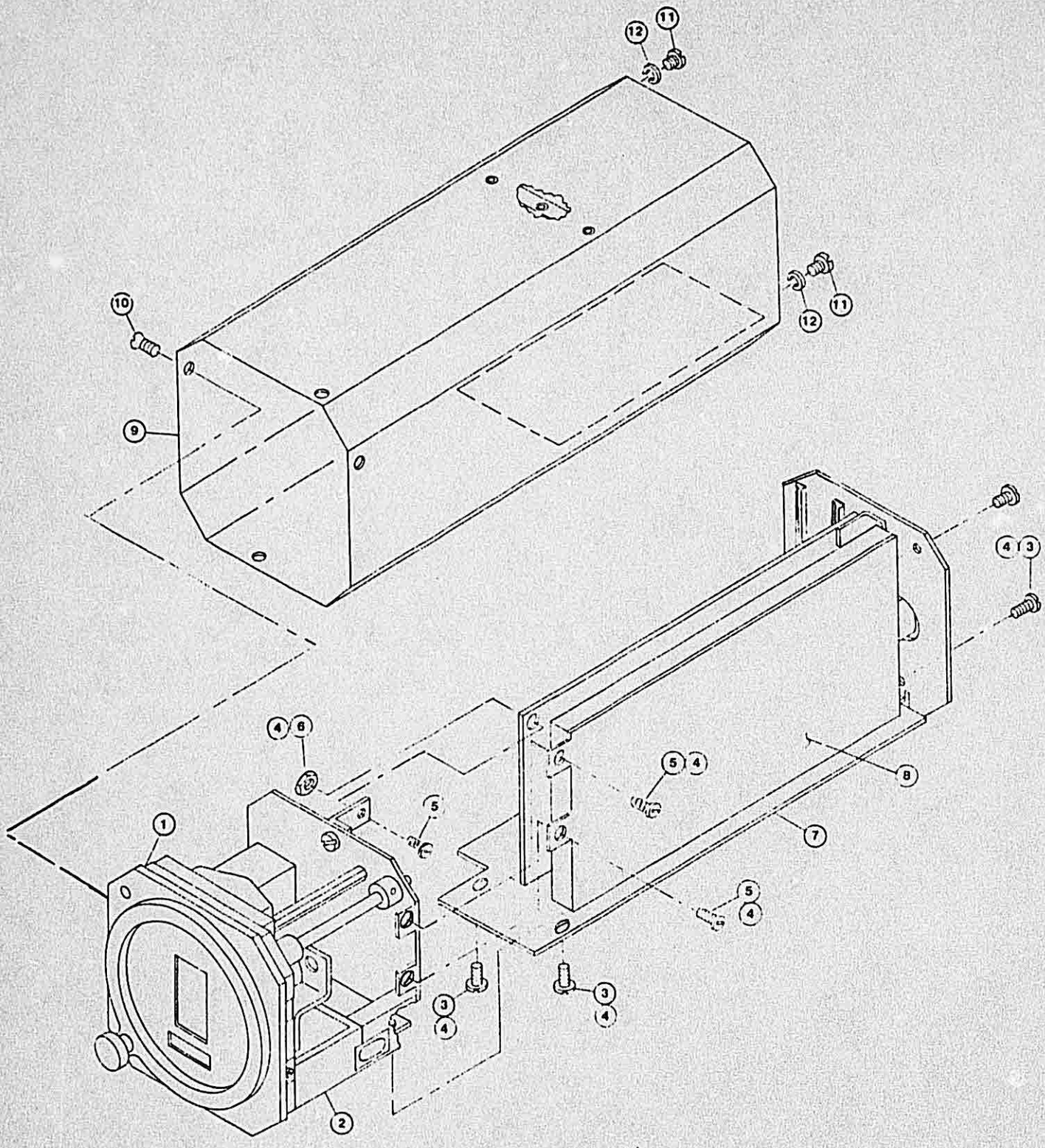


FIGURE 6-1 IDME 891 "T" BOARD & TRANSMITTER TO CONTROL HEAD MOUNTING

MECHANICAL PARTS LIST

FIGURE 6-1 IDME 891 "T" BOARD & TRANSMITTER TO CONTROL HEAD MOUNTING

ITEM	PART NO.	
1	56159-0001	Bezel Gasket
2	- - - - -	Control Head Assy. See Figure 6-3 for breakdown
3	82869-0702	Screw, Pan Hd Ph. #4-40x1/4
4	82802-0003	Washer, Lock #4 Internal Tooth
5	84536-0703	Screw, Pan Hd. Ph.#4-40x1/4
6	82900-0704	Nut, #4
7	- - - - -	"T" Board Assy.(includes bottom interconnect board and vertical range board) NOT PROCURABLE
8	01423-1390	Transmitter/Exciter Assy. (Complete & tested)
9	50718-0101	IDME 891 Case
10	82845-0302	Screw, Flt Hd 2-56x3/16
11	82814-0003	Screw, Bnd Hd #4-40x1/4
12	81324-0004	Washer, Lock #4

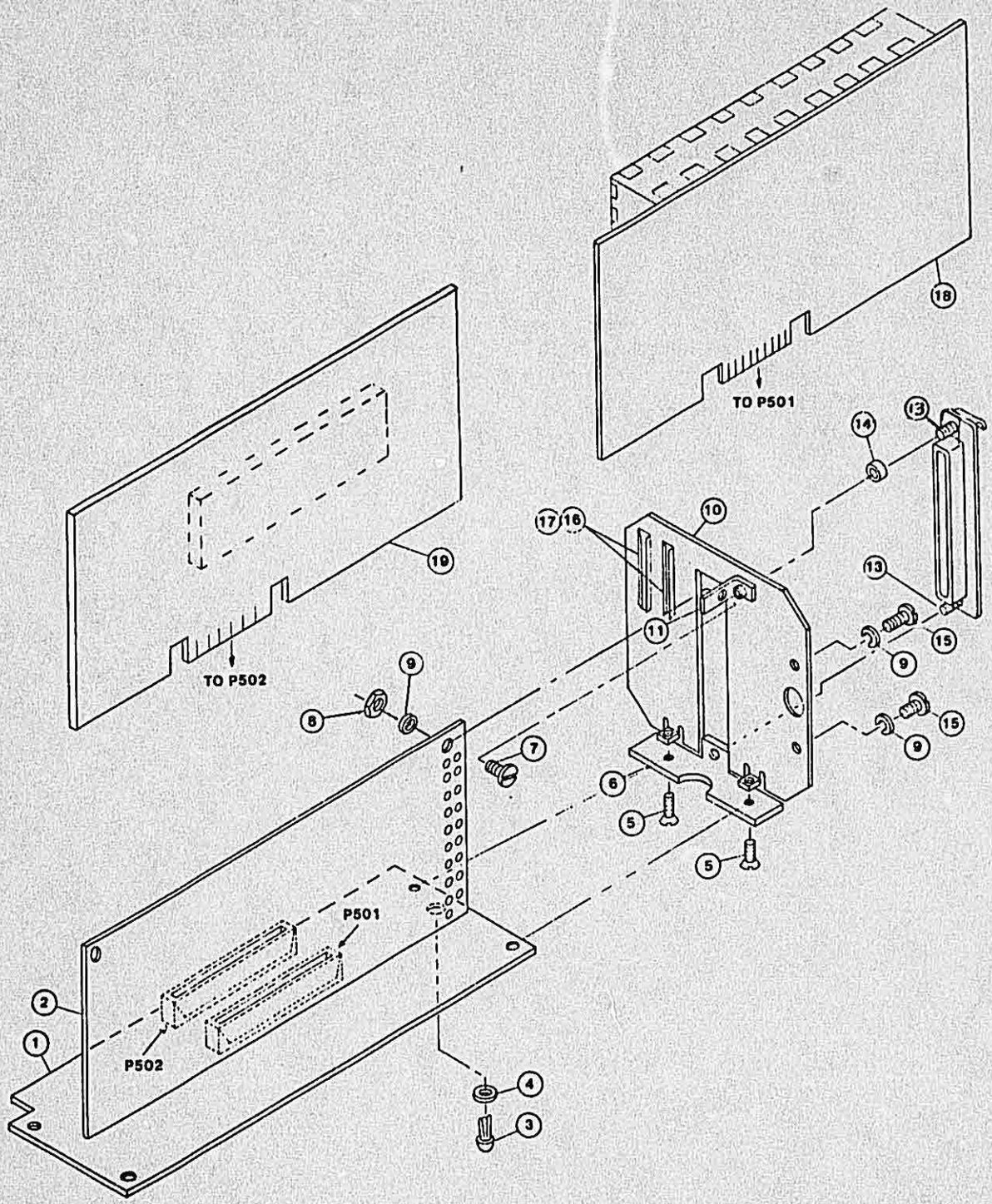


FIGURE 6-2 REAR PLATE TO "T" BOARD ASSY.

MECHANICAL PARTS LIST

FIGURE 6-2 IDME 891 REAR PLATE TO "T" BOARD ASSY. REF

ITEM	PART NO.	DESCRIPTION
1	- - - - -	Bottom Interconnect Board. NOT PROCURABLE
2	- - - - -	Range Board. NOT PROCURABLE
3	81366-0001	Plastic Split Rivet
4	81336-0025	Plastic Washer
5	84537-0703	Screw, Flt Hd #4-40x1/4
6	50727-0001	Connector Bracket
7	84536-0703	Screw, Pan Hd Ph. #4-40x1/4
8	82900-0704	Nut, #4
9	82802-0003	Washer, Lock #4 Internal Tooth
10	50725-0101	Rear Plate Assy.
11	56188-0102	Bracket
12	41355-0007	37 Pin Connector
13	41308-0006	Connector Locking Assy.
14	81206-0188	Spacer (.050)
15	82869-0702	Screw, Pan Hd Ph. #4-40x1/4
16	84177-0001	PC Board Retainer
17	81254-0052	Eyelets
18	01427-1390	IF Receiver/Power Supply Board (Complete & tested)
19	01426-1390	VCO/SYNTH Board (Complete & tested)

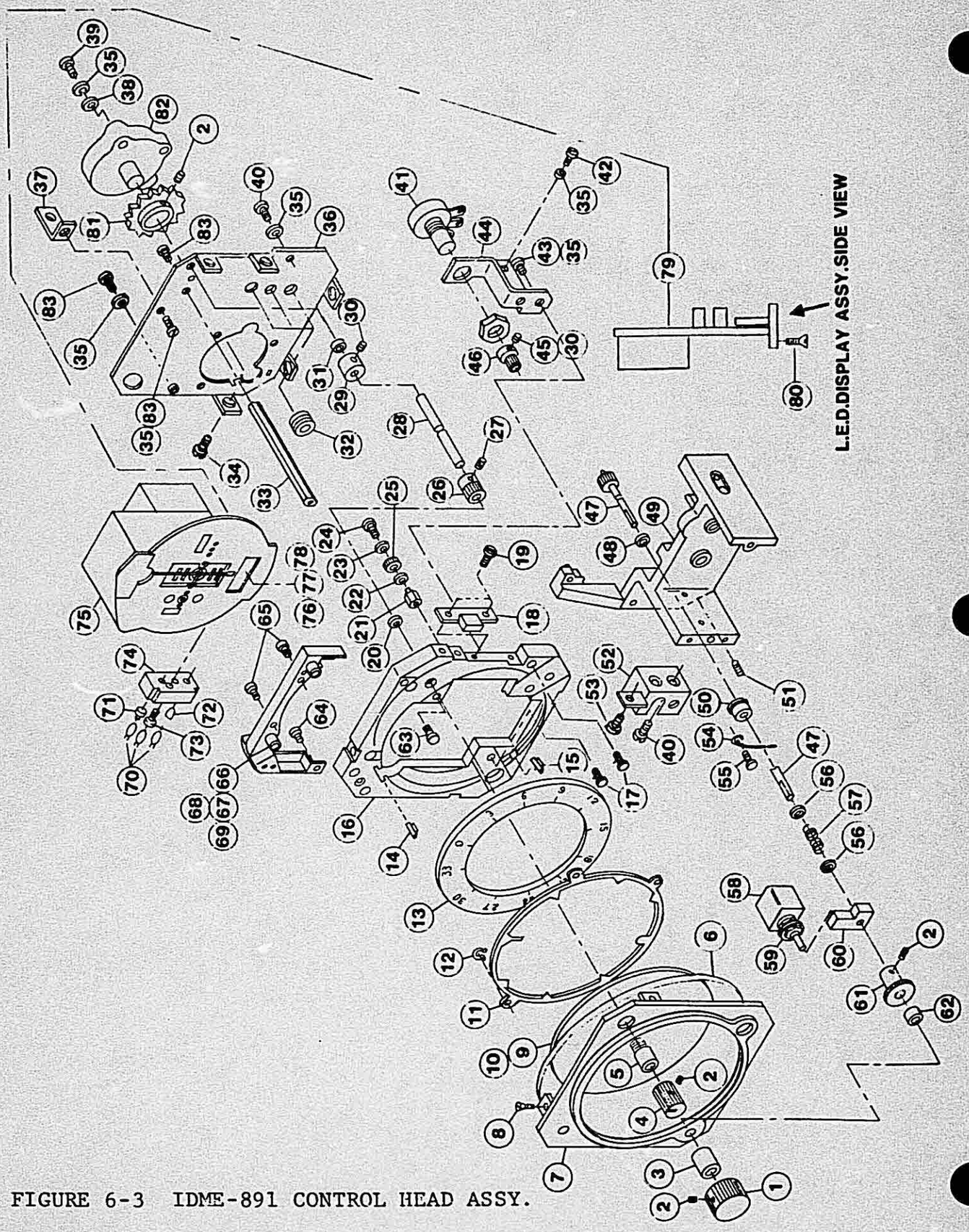
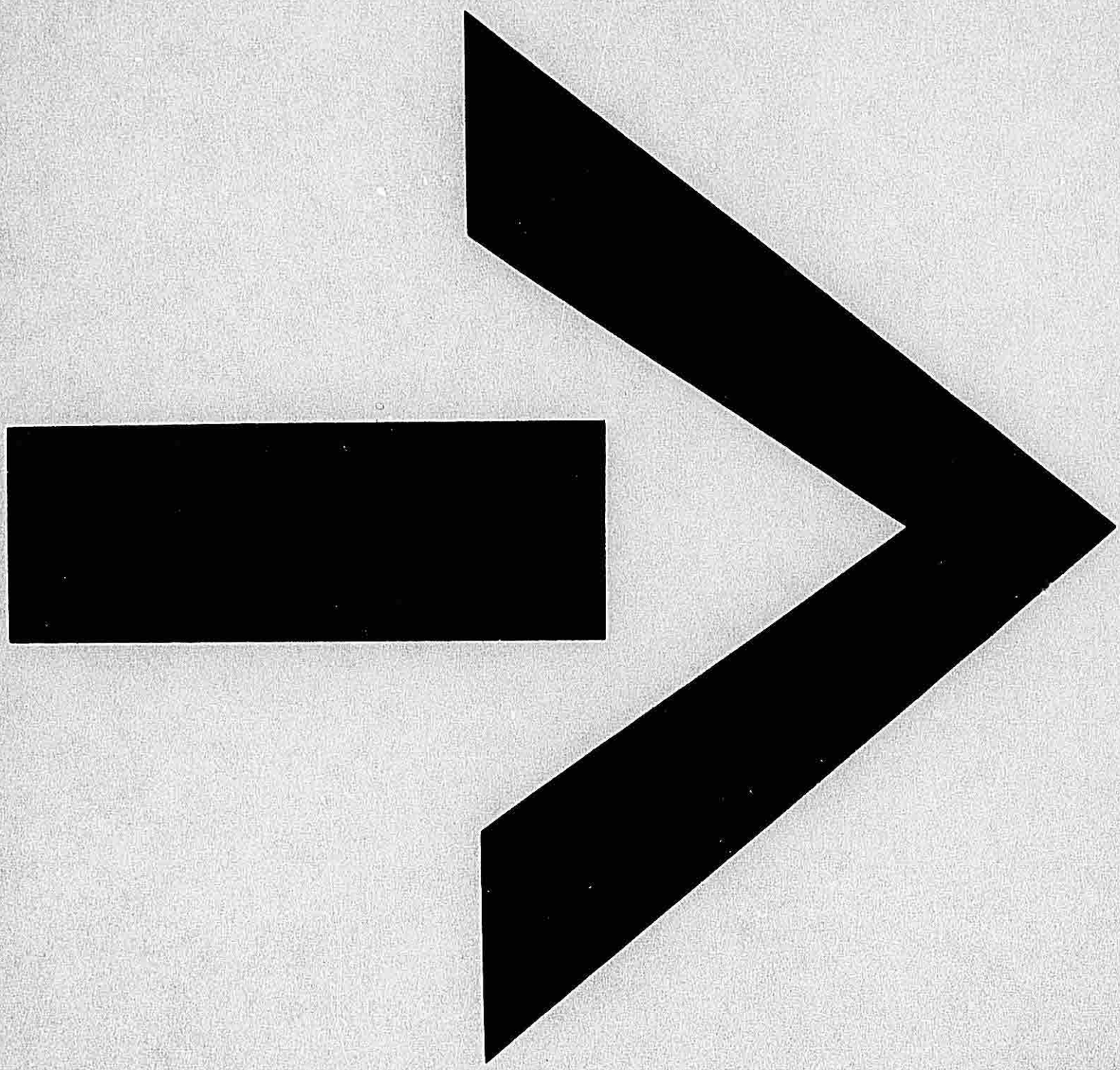


FIGURE 6-3 IDME-891 CONTROL HEAD ASSY.



MECHANICAL PARTS LIST

FIGURE 6-3 IDME 891 CONTROL HEAD ASSY. REF

ITEM	PART NO.	DESCRIPTION
1	88227-0001	Knob, OBS
2	82863-0219	Screw, Set, #4-40x3/32
3	88230-0001	Spacer, Knob
4	88228-0001	Knob
5	55995-0002	Bushing, Front Panel
6	56159-0001	Rubber Gasket
7	56059-0020	Bezel, IDME 891
8	82884-0503	Screw, Flt Hd Ph. Und. #4-40x1/4
9	50252-0002	Wedge, Lens
10	99065-0008	Tape, Double Sided
11	56914-0001	Mask, Bezel
12	81192-0014	Ring, Retaining
13	56911-0001	Azimuth, Card
14	56908-0002	Guide, Dial, Fixed
15	56908-0001	Guide, Dial, Fixed
16	56025-0004	Casting, Front
17	82965-0702	Screw, Fil Hd Ph. #4-40x3/16
18	01425-1325	Spring Guide Assy.
19	84533-0702	Screw, Pn Hd Ph. #2-56x3/16
20	81307-0134	Flat Washer (Steel)
21	56030-0001	Spacer, Idler
22	81307-0133	Flat Washer (Brass)
23	81324-0002	Washer, Lock #2
24	84533-0707	Screw, Pn Hd Ph. #2-56x1/2
25	56032-0001	Idler Gear
26	56053-0001	Gear, Pinion
27	82863-0204	Screw, Set, #2-56x1/16
28	56055-0001	Shaft On/Off Ident
29	56042-0001	Collar
30	82863-0204	Screw, Set, #2-56x1/16
31	81206-0164	Spacer
32	81160-0014	Rubber Grommet
33	81207-0049	Spacer Hex
34	84537-0703	Screw, Flt Hd #4-40x1/4 (Undercut)
35	81324-0004	Washer, Lock #4
36	50726-0101	Mid Plate Assembly
37	56188-0102	Bracket
38	81329-0004	Washer, Flat #4
39	82869-0707	Screw, Pn Hd Ph. #4-40x3/4
40	82884-0503	Screw, Flt Hd Ph. Und. #4-40x1/4
41	32070-0007	Resistor, Variable W/Switch
42	84536-0704	Screw, Pn Hd Ph. #4-40x5/16
43	84536-0702	Screw, Pn Hd Ph. #4-40x3/16
44	56049-0001	Bracket Vol-On-Off
45	82863-0202	Screw, Set, #2-56x3/32
46	56031-0001	Pinion, Gear

FIGURE 6-3 IDME 891 CONTROL HEAD ASSY., Continued REF

ITEM	PART NO.	DESCRIPTION
47	56056-0101	Gear and Shaft Assembly, OBS Dial
48	81206-0117	Spacer
49	56026-0002	Casting Rear
50	81335-0017	Bushing (Insulator)
51	82863-0205	Screw, Set, #2-56x5/32
52	56047-0001	Bracket Switch
53	82965-0703	Screw, Fil Hd Ph. #4-40x1/4
54	56114-0001	Spring, OBS Shaft
55	82814-0402	Screw, Bnd Hd Sl. #4-40x3/16
56	81807-0134	Washer
57	56034-0001	Spring Actuator
58	61576-0002	Switch, Push Button, D.P.D.T.
59	81369-0001	Washer, Open End
60	56046-0001	Switch Actuator
61	56906-0101	Gear, OBS
62	56907-0001	OBS Bearing
63	82807-0704	Screw, Flt Hd Ph. #2-56x5/16
64	84533-0702	Screw, Pn Hd Ph. #2-56x3/16
65	82808-0706	Screw, Rd Hd Ph. #2-56x7/16
66	56085-0001	Light Block, Pilot Lights
67	81456-0005	Standoff, Pilot Lights
68	81747-0015	Filter Lamp, Blue
69	12000-0032	Lamp, 8640, Pilot
70	12009-0002	Lamp, Pin Base, Marker DS909
70	12009-0002	Lamp, Pin Base, Marker DS910
70	12009-0004	Lamp, Pin Base, Marker DS911
71	12009-0001	Socket, Miniature Marker
72	81747-0009	Filter, Colored (Blue) Marker
73	82972-0004	Screw, Fil Hd Sl. #2-56x1/4
74	56082-0001	Light Block
75	76133-0001	Meter Assembly
76	82994-0004	Screw, Truss Hd Sl. #0-80x1/8
77	50729-0001	Lens Filter, DME Readout
78	82916-0001	Hex Nut #0-80
79	01425-1360	L.E.D Display Assy. (includes 4 L.E.D's, bracket, and P.C. Board)
80	82807-0702	Screw, Flt Hd Ph. #2-56x3/16
81	56057-0001	Gear, OBS Pot
82	32068-0001	Potentiometer, Variable, OBS
83	82804-0703	Screw, Rd Hd Ph. #4-40x1/4

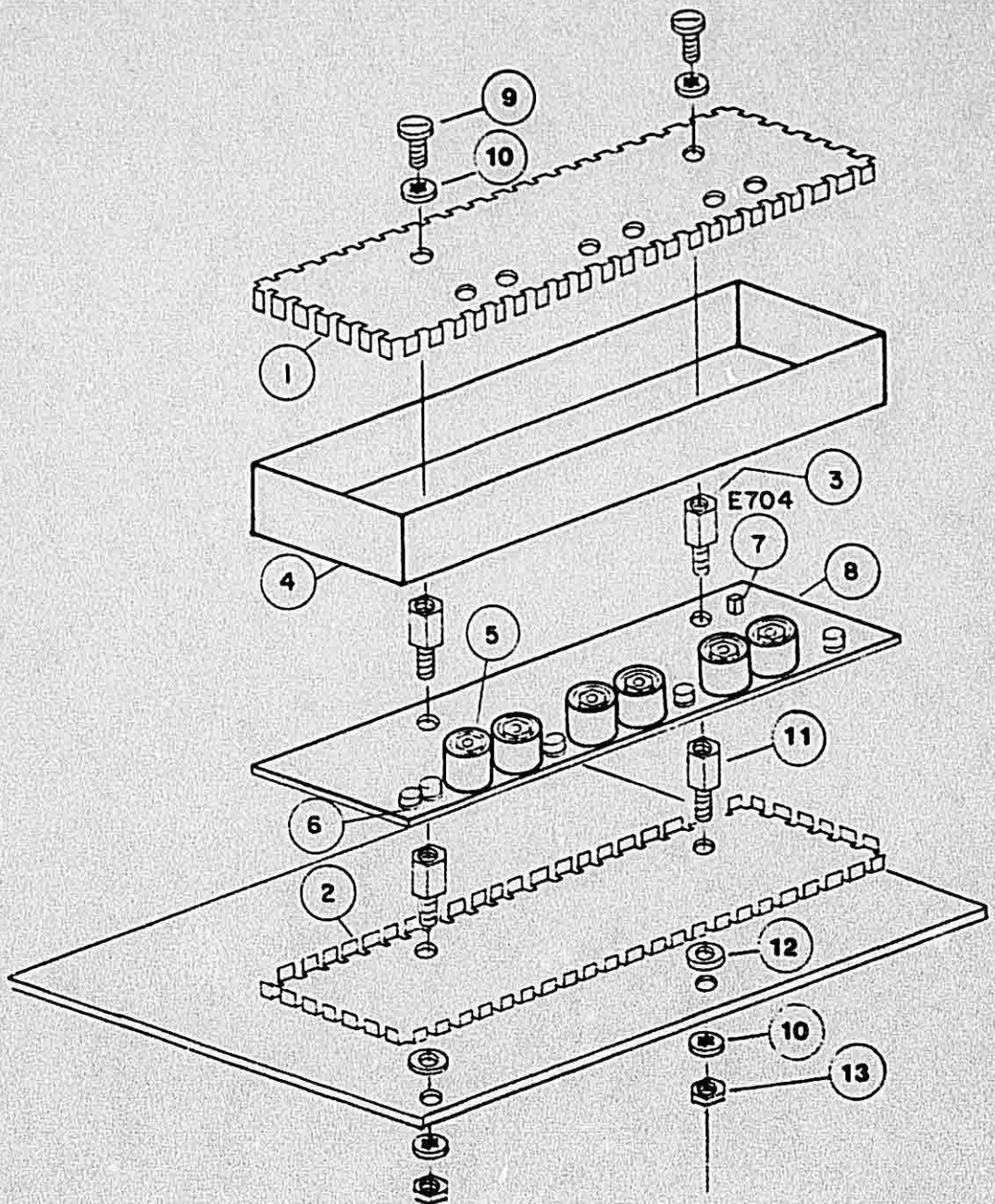
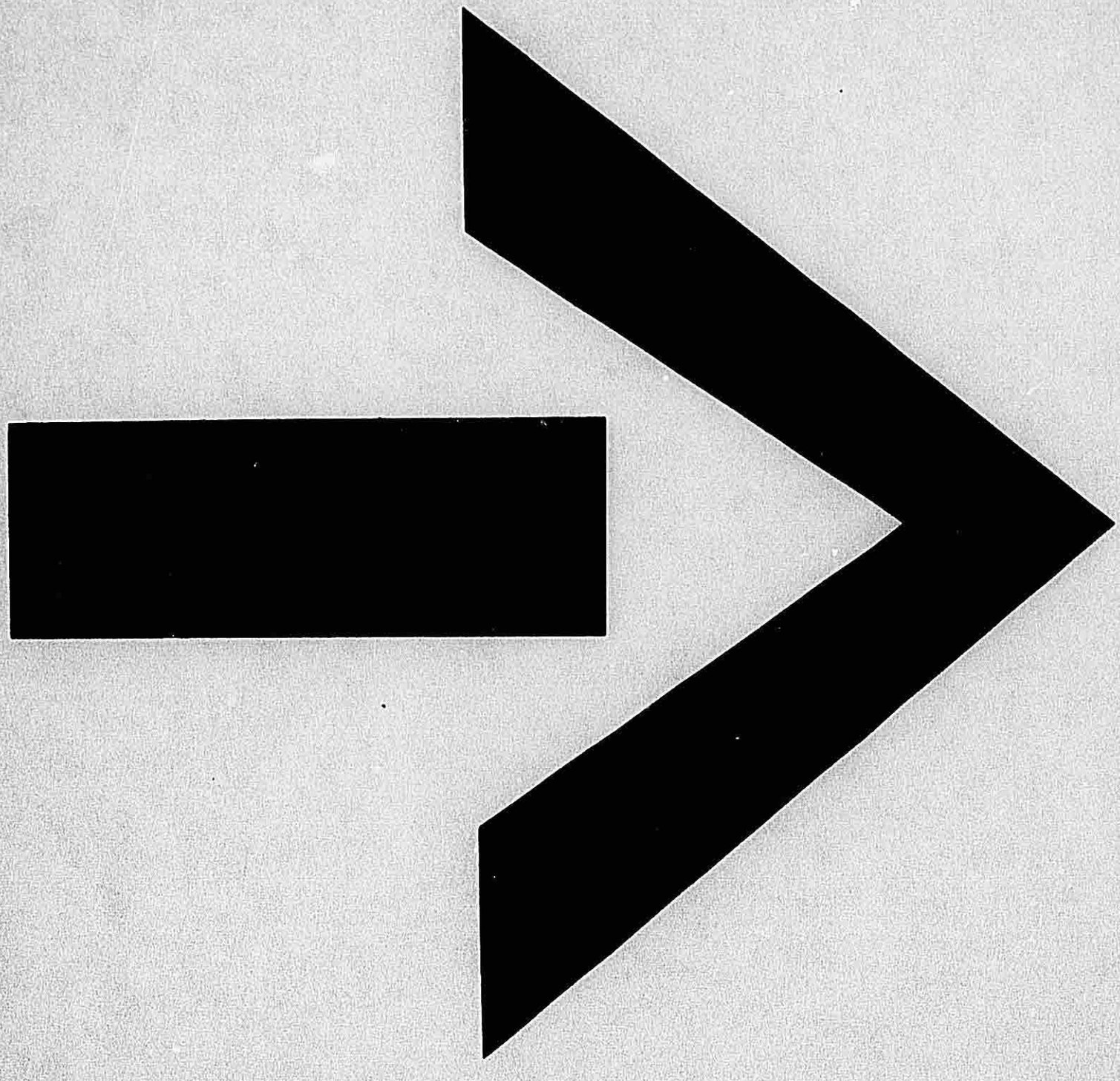


FIGURE 6-4 IF RECEIVER MECHANICAL ASSY.



MECHANICAL PARTS LIST

FIGURE 6-4 IF RECEIVER ASSY. REF.

ITEM	PART NO.	DESCRIPTION
1	50022-0001	Top Cover
2	50022-0002	Bottom Cover
3	81342-0015	Threaded Spacer
4	50021-0001	Wraparound Shield
5	50038-0001	IF Coil Shield
6	83037-0002	Transistor Mounting Pad
7	81808-0104	Square Post Terminal
8	50027-0001	P.C. Board (Less components)
9	82892-0402	Screw, Pan hd. #4-40x3/16
10	82802-0703	Lockwasher, #4, Internal Tooth
11	81342-0016	Threaded Spacer
12	81312-0016	Spring Washer
13	82900-0704	Nut, #4-40

NOTE: The IF receiver is part of the IF receiver/power supply board. The whole complete & tested board is available as an exchange module. The order number is 01427-1390.

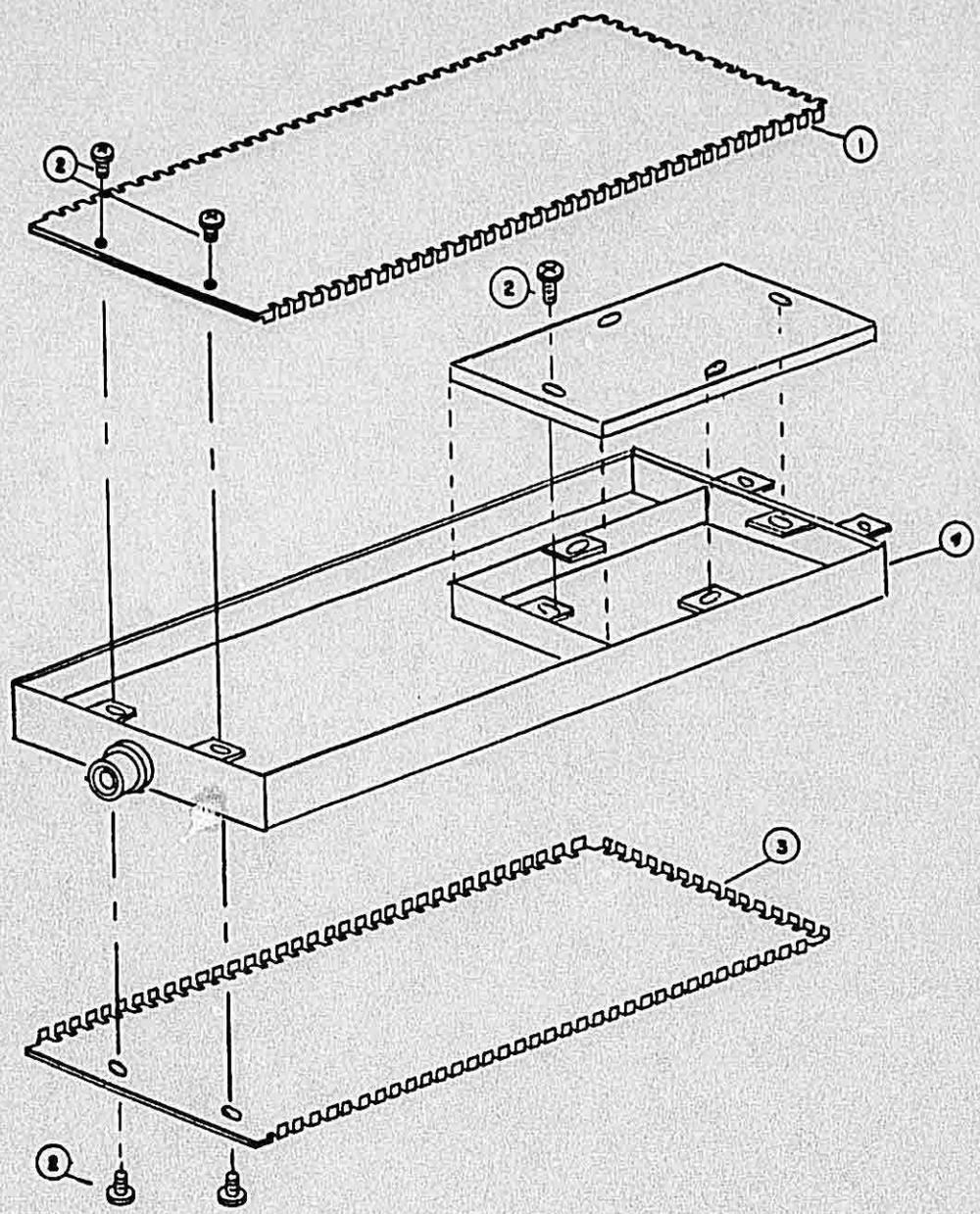
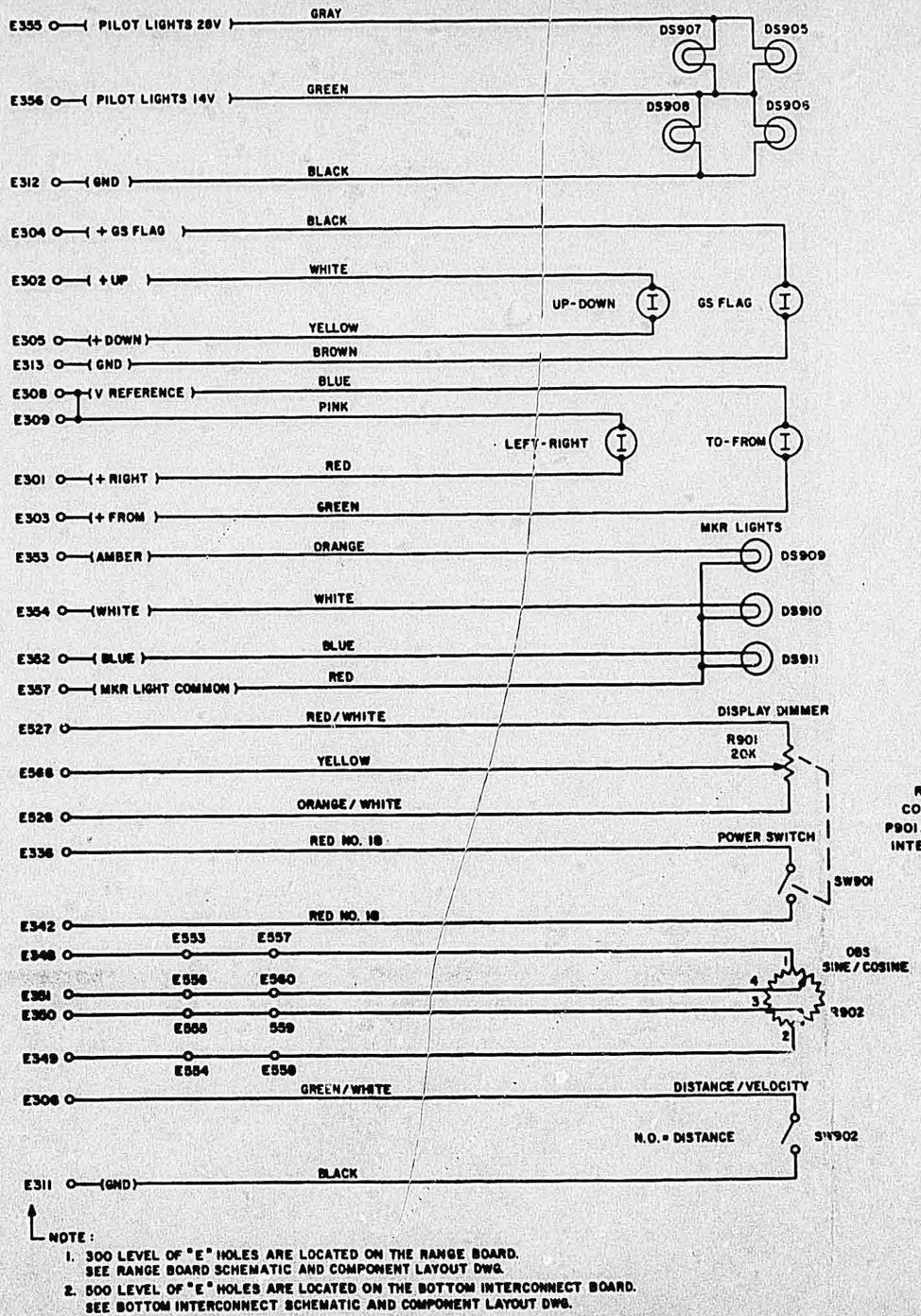


FIGURE 6-5 TRANSMITTER MECHANICAL ASSY.

ITEM	PART NO.	DESCRIPTION
1	50722-0001	Top Cover
2	84542-0701	Screw, Taptite Pan Hd. #2-56x1/8
3	50722-0001	Bottom Cover (Same as top cover)
4	01423-1390	Transmitter/Exciter Assy. (Complete & tested)
5	50721-0001	Exciter Cover



NOTE:
1. 300 LEVEL OF "E" HOLES ARE LOCATED ON THE RANGE BOARD. SEE RANGE BOARD SCHEMATIC AND COMPONENT LAYOUT DWG.
2. 500 LEVEL OF "E" HOLES ARE LOCATED ON THE BOTTOM INTERCONNECT BOARD. SEE BOTTOM INTERCONNECT SCHEMATIC AND COMPONENT LAYOUT DWG.

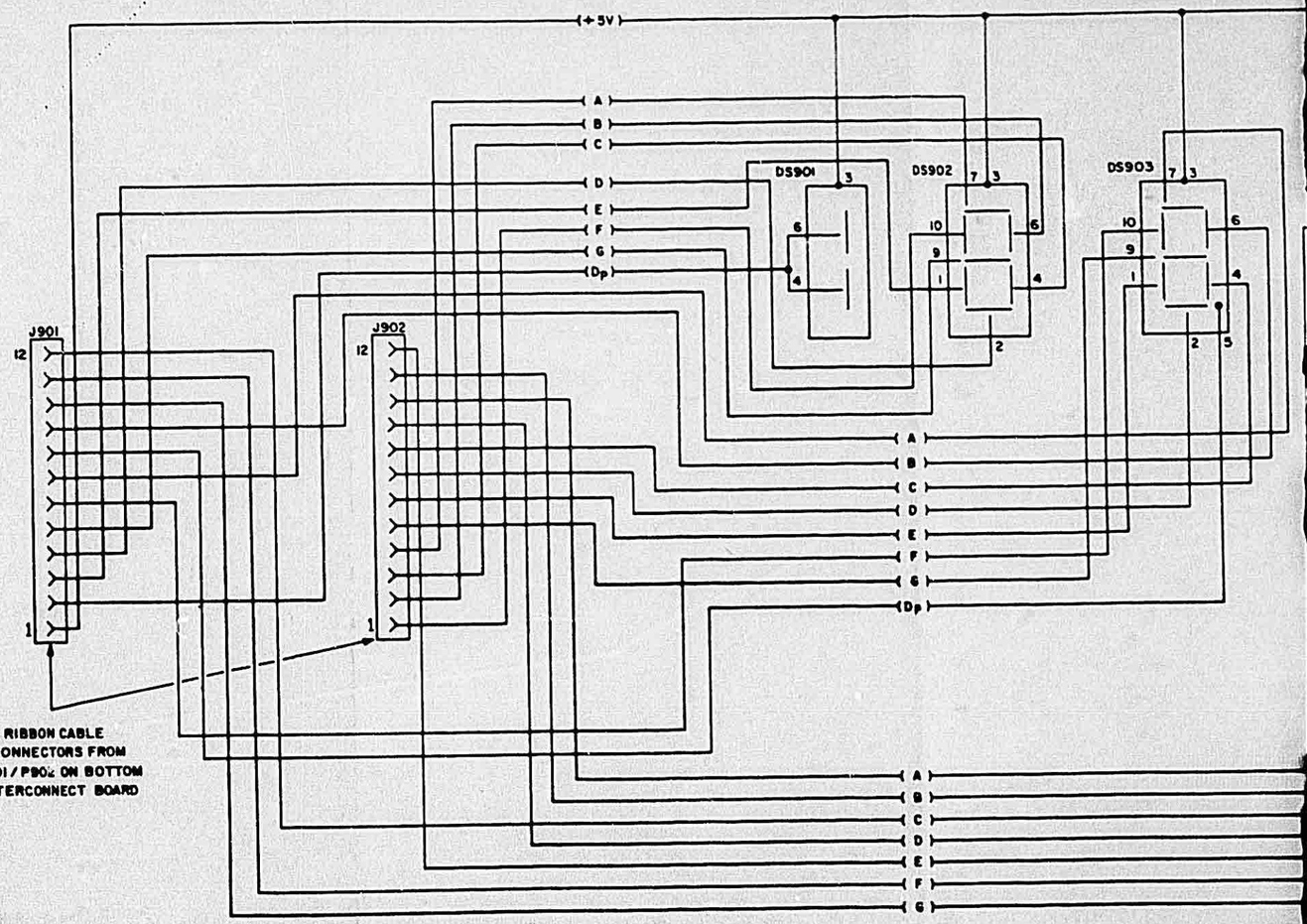
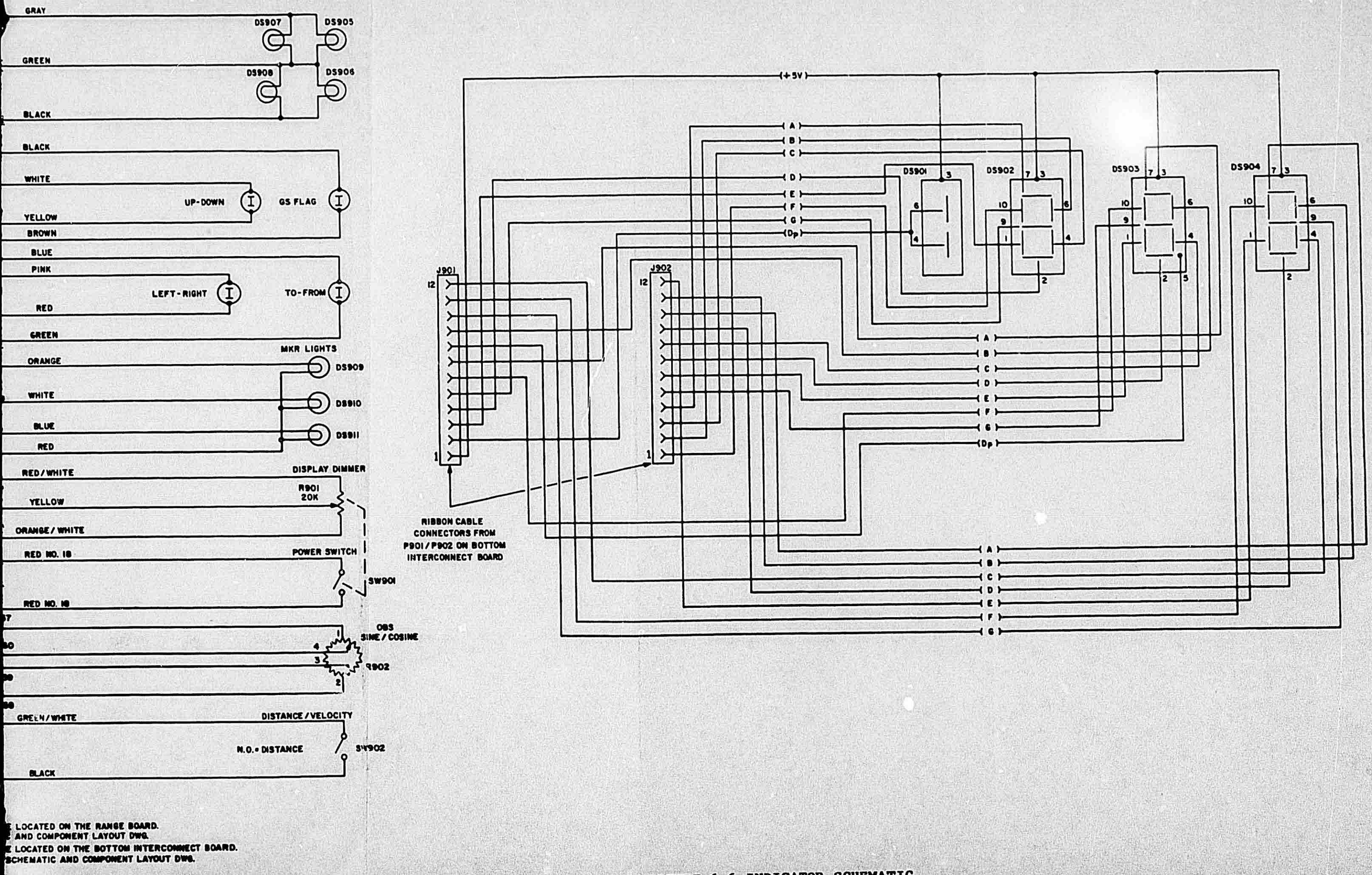
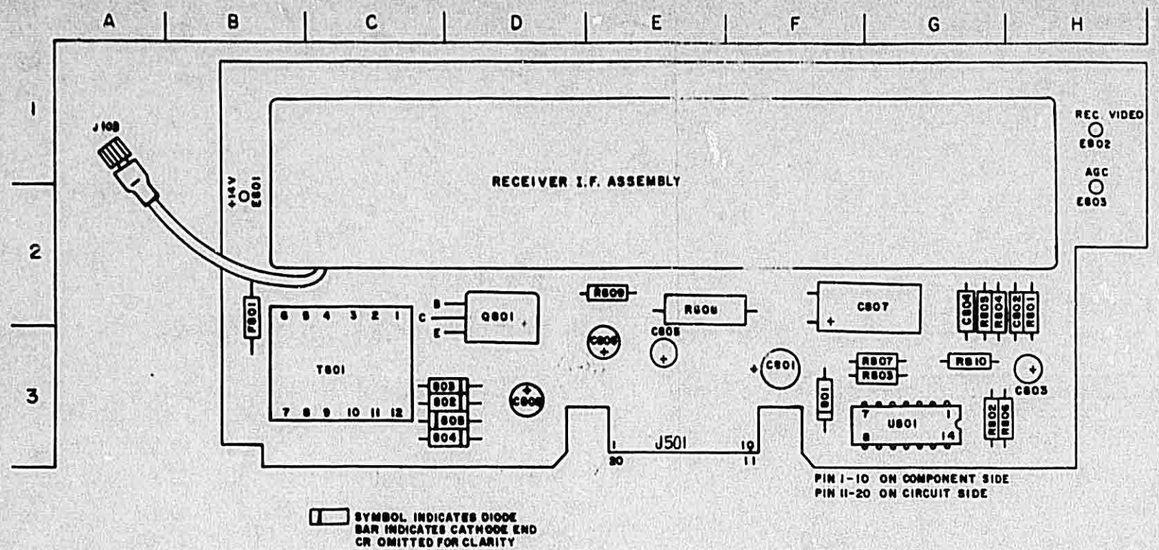


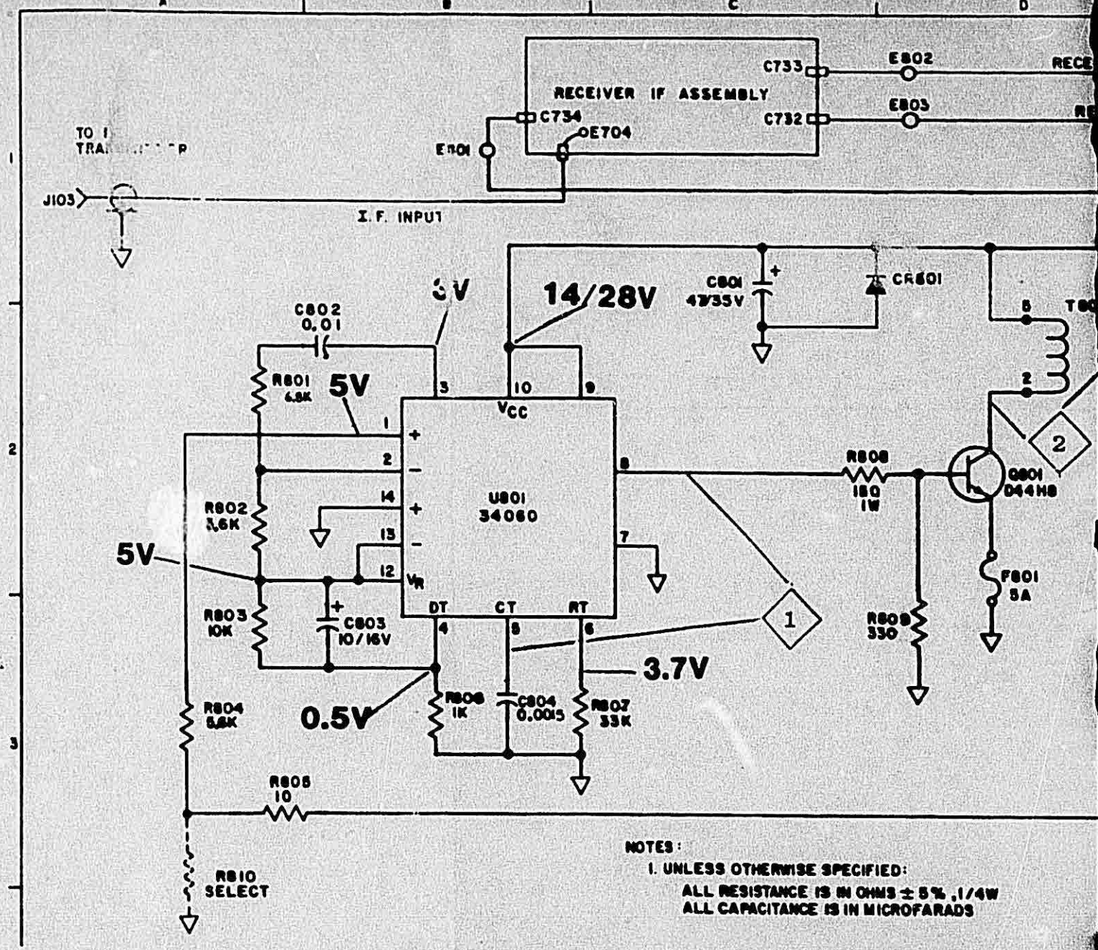
FIGURE 6-6 INDICATOR SCHEMATIC



LOCATED ON THE RANGE BOARD.
AND COMPONENT LAYOUT DWG.
LOCATED ON THE BOTTOM INTERCONNECT BOARD.
SCHEMATIC AND COMPONENT LAYOUT DWG.

FIGURE 6-6 INDICATOR SCHEMATIC





IDME 891 POWER SUPPLY ELECTRICAL PARTS LIST
BM 01427-101

Action	Chassis Level Code	Symbol	PART NUMBER	DESCRIPTION	Grid Coordinates Schematic	Component Assy
O	B	C801	21564-0169	Cap., Tant., 47uF ±10%, 35V	F3	C1
O	B	C802	24565-0028	Cap., Ceramic, 0.01uF ±10%, 50V	H2	B2
O	B	C803	21567-0011	Cap., Elect. 10uF, ±20%, 16V	H3	B3
O	B	C804	24566-0039	Cap., Ceramic, 0.0015 uF ±5%, 50V	G2	B3
O	B	C805	21567-0024	Cap., Elect., 4.7uF +75-10%, 100V	E3	E2
O	B	C806	21567-0028	Cap., Elect., 220uF ±20%, 25V	E3	E2
O	B	C807	21567-0037	Cap., Elect., 220uF ±20%, 25V	G2	E2
O	B	C808	21567-0028	Cap., Elect., 220uF ±20%, 25V	D3	E2
O	B	CR801	75204-0045	Diode, Silicon	F3	C1
O	B	CR802	75216-0003	Diode, Silicon, 300V 1N4935	C3	E2
O	B	CR803	75216-0003	Diode, Silicon, 300V 1N4935	C3	E2
O	B	CR804	75216-0003	Diode, Silicon, 300V 1N4935	C3	E2
O	B	CR805	75216-0003	Diode, Silicon, 300V 1N4935	C3	E2
O	B	J103	41244-0001	Connector, RF, Min., Screw On	A1	A1
O	B	R801	31218-0682	Resistor, Carbon, Film, 6.8K ±5% 1/4w	H2	A2
O	B	R802	31218-0562	Resistor, Carbon, Film, 5.6K ±5% 1/4w	G3	A2
O	B	R803	31218-0103	Resistor, Carbon, Film, 10K ±5% 1/4w	G3	A3
O	B	R804	31218-0562	Resistor, Carbon, Film, 5.6K ±5% 1/4w	G2	A3
O	B	R805	31218-0100	Resistor, Carbon, Film, 10 ±5% 1/4w	G2	A3
O	B	R806	31218-0102	Resistor, Carbon, Film, 1K ±5% 1/4w	G3	B3
O	B	R807	31218-0333	Resistor, Carbon, Film, 33K ±5% 1/4w	G3	B3
O	B	R808	31150-0151	Resistor, Fixed Comp. 150 ±5% 1w	E2	D2
O	B	R809	31218-0331	Resistor, Carbon, Film, 330 ±5% 1/4w	E2	D3
O	B	R810	31218-SEL	Resistor, Carbon, Film, Slect By Test	G3	A3
O	B	F801	66516-0001	Fuse, Sub-Mineature, 125V, 5A	B2	D2
O	B	Q801	75812-0004	Transistor, Power, D-44H8	D2	D2
O	B	T801	11961-0001	Transformer	C3	D2
O	B	U801	74245-0001	Intergrated Circuit, 34060	G3	B2

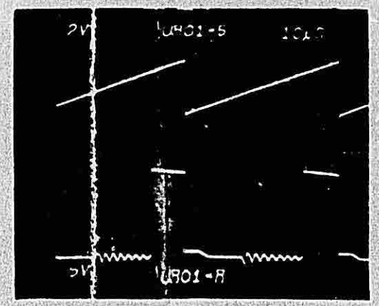
OSCILLOSCOPE MAIN TRIGGERING

MODE: NORM (Trigger)
COUPLING: DC
SOURCE: INTERNAL
DISPLAY MODE: ALTERNATE
PROBE COUPLING: AC

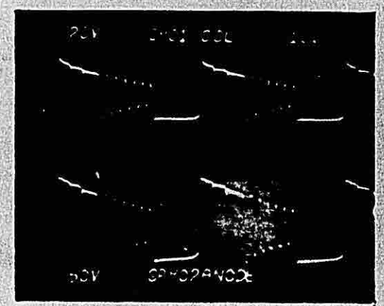
WAVEFORM NOTES

The waveform photographs provide the following information:

1. Scope Vertical Scale (volts/div).
   In the upper left corner of the photograph is displayed the volts/div for the upper trace. In the lower left corner is displayed the volts/div for the lower trace.
2. Scope Horizontal Scale (time/div)
   In the upper right corner of the photograph is displayed the time/div for **BOTH** the upper and bottom traces.
3. Test Points
   The top center edge of the photograph identifies the test point for the upper trace. The bottom center edge identifies the test point for the bottom trace.
4. Each waveform is identified by a numbered diamond, which correlates with a numbered diamond found in the schematic.

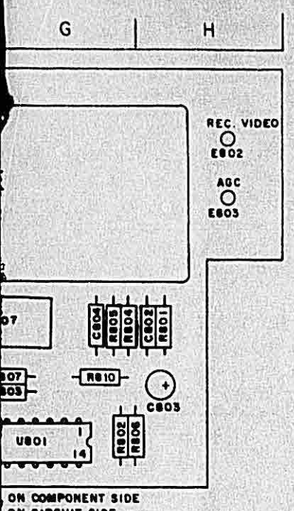


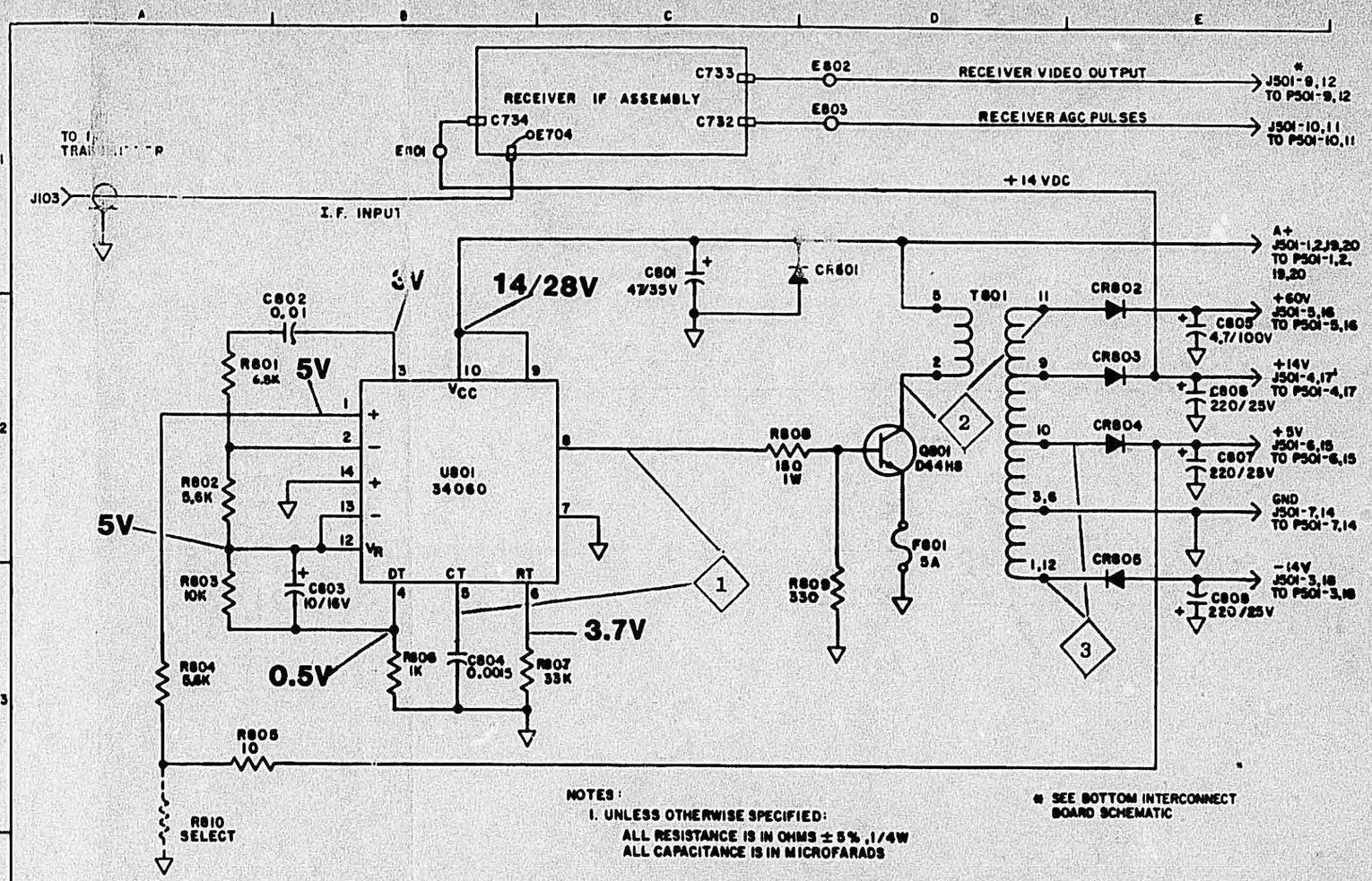
1



2

FIGURE 6-7 POWER SUPPL





OSCILLOSCOPE MAIN TRIGGERING

MODE: NORM (Trigger)
COUPLING: DC
SOURCE: INTERNAL
DISPLAY MODE: ALTERNATE
PROBE COUPLING: AC

NOTES:

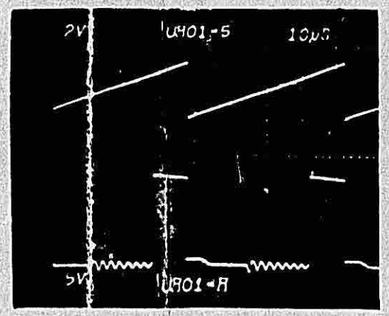
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IS IN OHMS ± 5%, 1/4W
   ALL CAPACITANCE IS IN MICROFARADS

* SEE BOTTOM INTERCONNECT BOARD SCHEMATIC

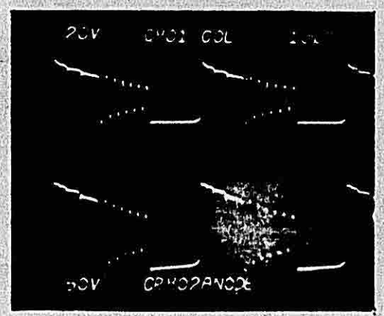
WAVEFORM NOTES

The waveform photographs provide the following information:

1. Scope Vertical Scale (volts/div).
   In the upper left corner of the photograph is displayed the volts/div for the upper trace. In the lower left corner is displayed the volts/div for the lower trace.
2. Scope Horizontal Scale (time/div)
   In the upper right corner of the photograph is displayed the time/div for BOTH the upper and bottom traces.
3. Test Points
   The top center edge of the photograph identifies the test point for the upper trace. The bottom center edge identifies the test point for the bottom trace.
4. Each waveform is identified by a numbered diamond, which correlates with a numbered diamond found in the schematic.



1



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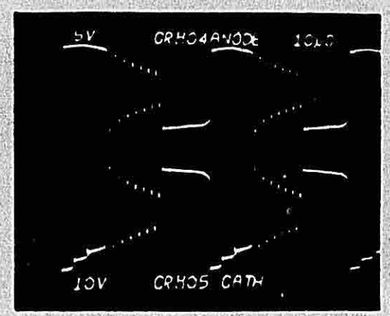
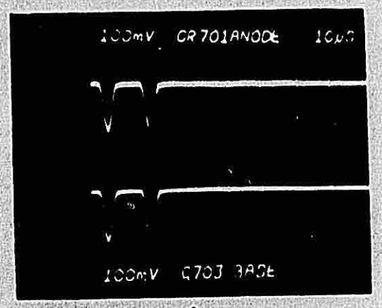


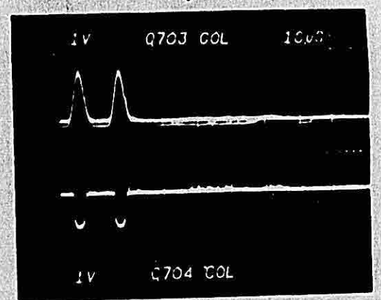
3

FIGURE 6-7 POWER SUPPLY SCHEMATIC



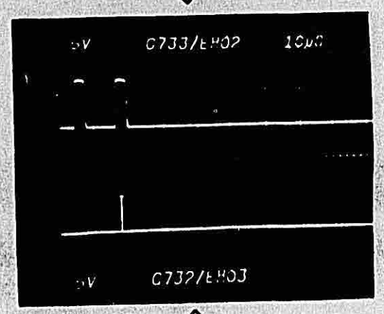
-72dBM SIGNAL AND BASE OF Q702 SHORTED TO GROUND

④



-78dBM SIGNAL

⑤

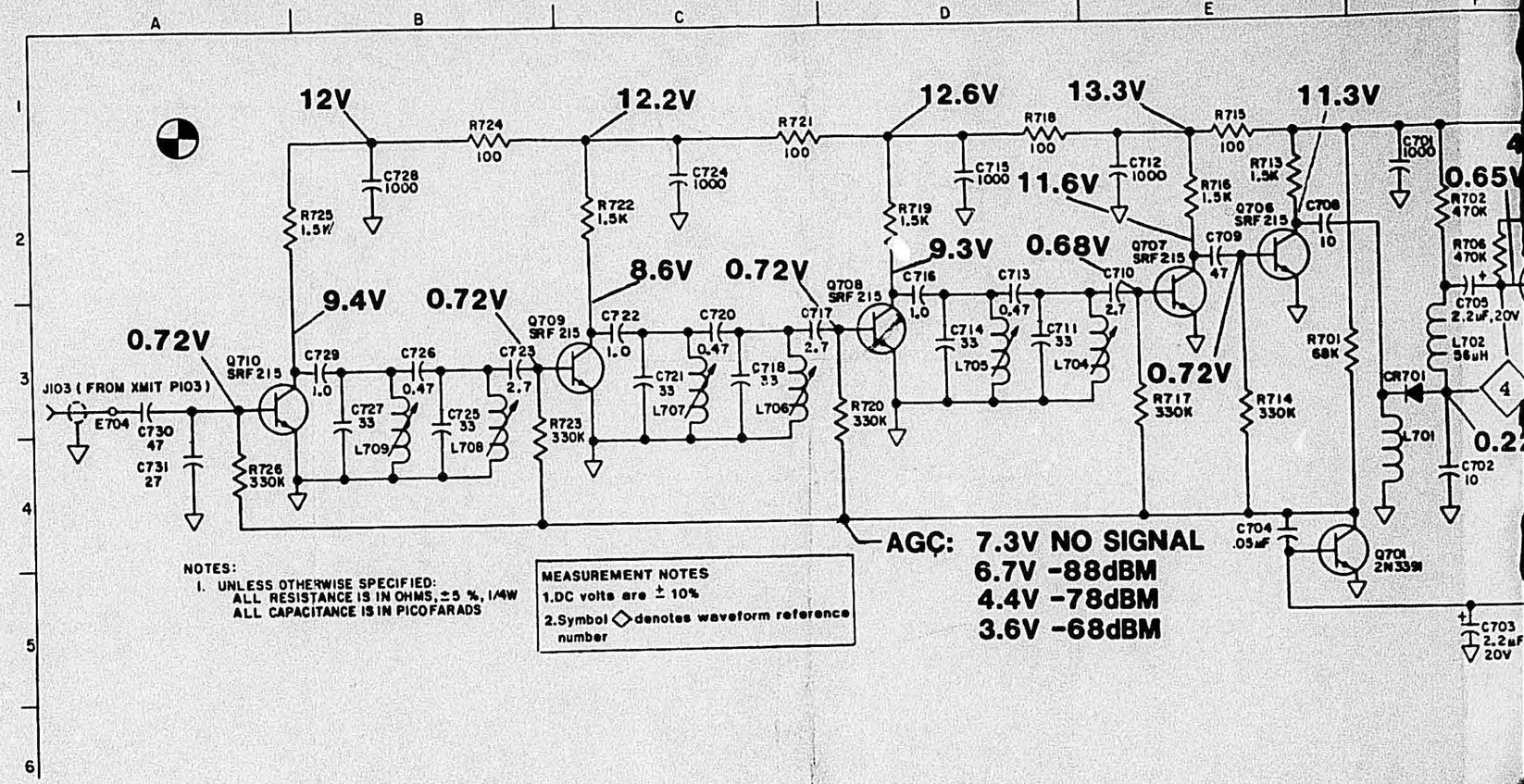


-78dBM SIGNAL

⑥

OSCILLOSCOPE MAIN TRIGGERING

MODE: NORM (Trigger)
COUPLING: DC
SOURCE: INTERNAL
DISPLAY MODE: ALTERNATE
PROBE COUPLING: AC



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IS IN OHMS, ±5 %, 1/4W
ALL CAPACITANCE IS IN PICOFARADS

MEASUREMENT NOTES
1. DC volts are ± 10%
2. Symbol ◇ denotes waveform reference number

WAVEFORM NOTES

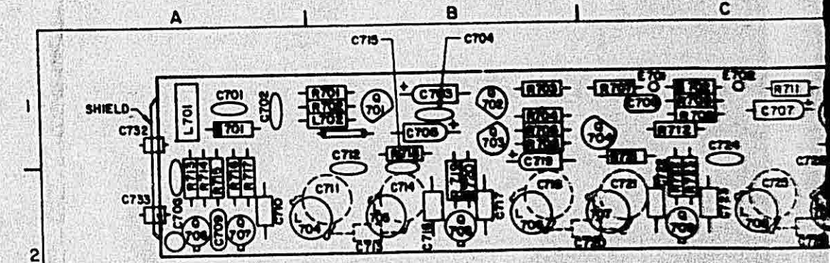
The waveform photographs provide the following information:

1. Scope Vertical Scale (volts/div).
In the upper left corner of the photograph is displayed the volts/div for the upper trace. In the lower left corner is displayed the volts/div for the lower trace.

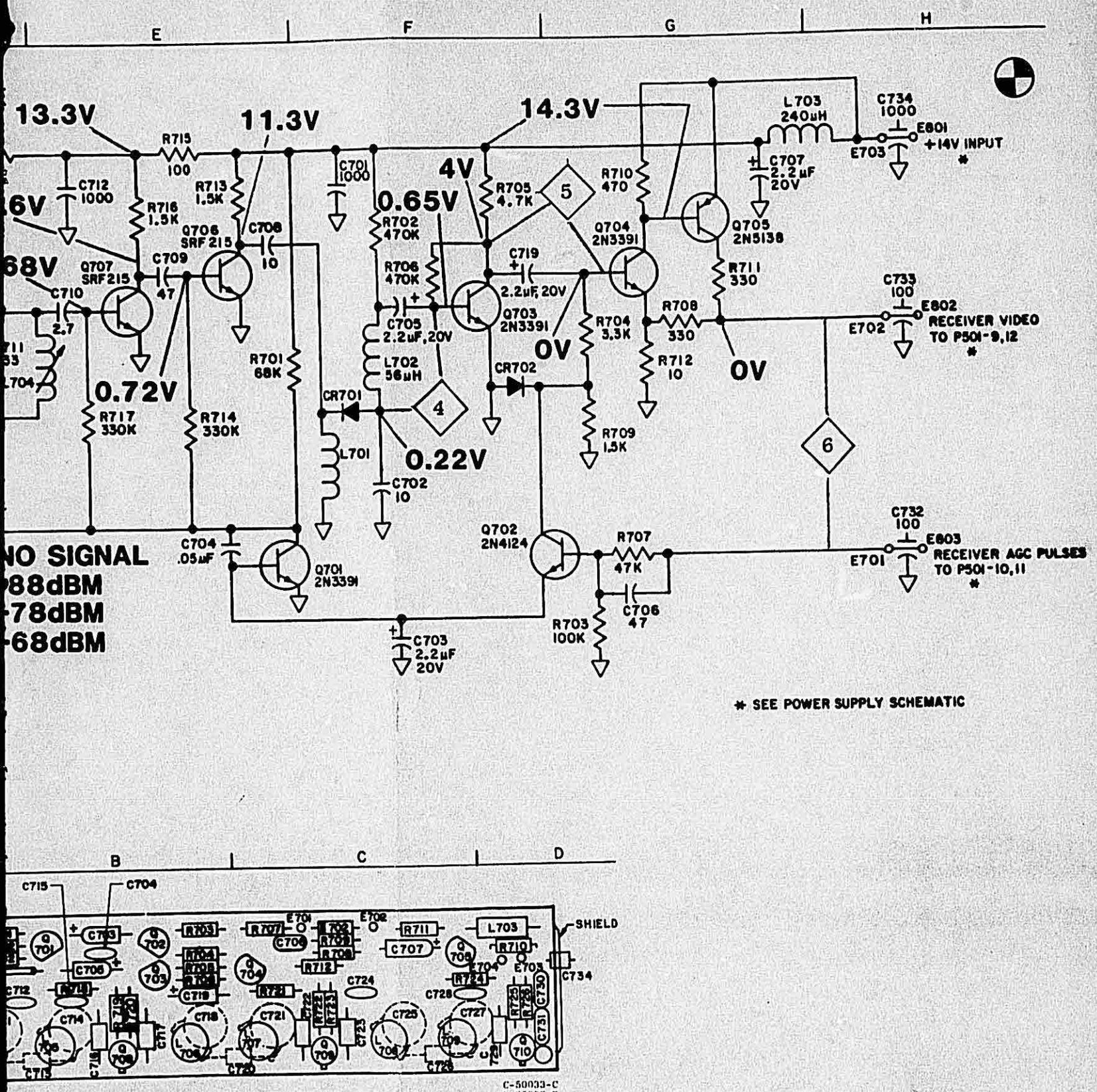
2. Scope Horizontal Scale (time/div)
In the upper right corner of the photograph is displayed the time/div for **BOTH** the upper and bottom traces.

3. Test Points
The top center edge of the photograph identifies the test point for the upper trace. The bottom center edge identifies the test point for the bottom trace.

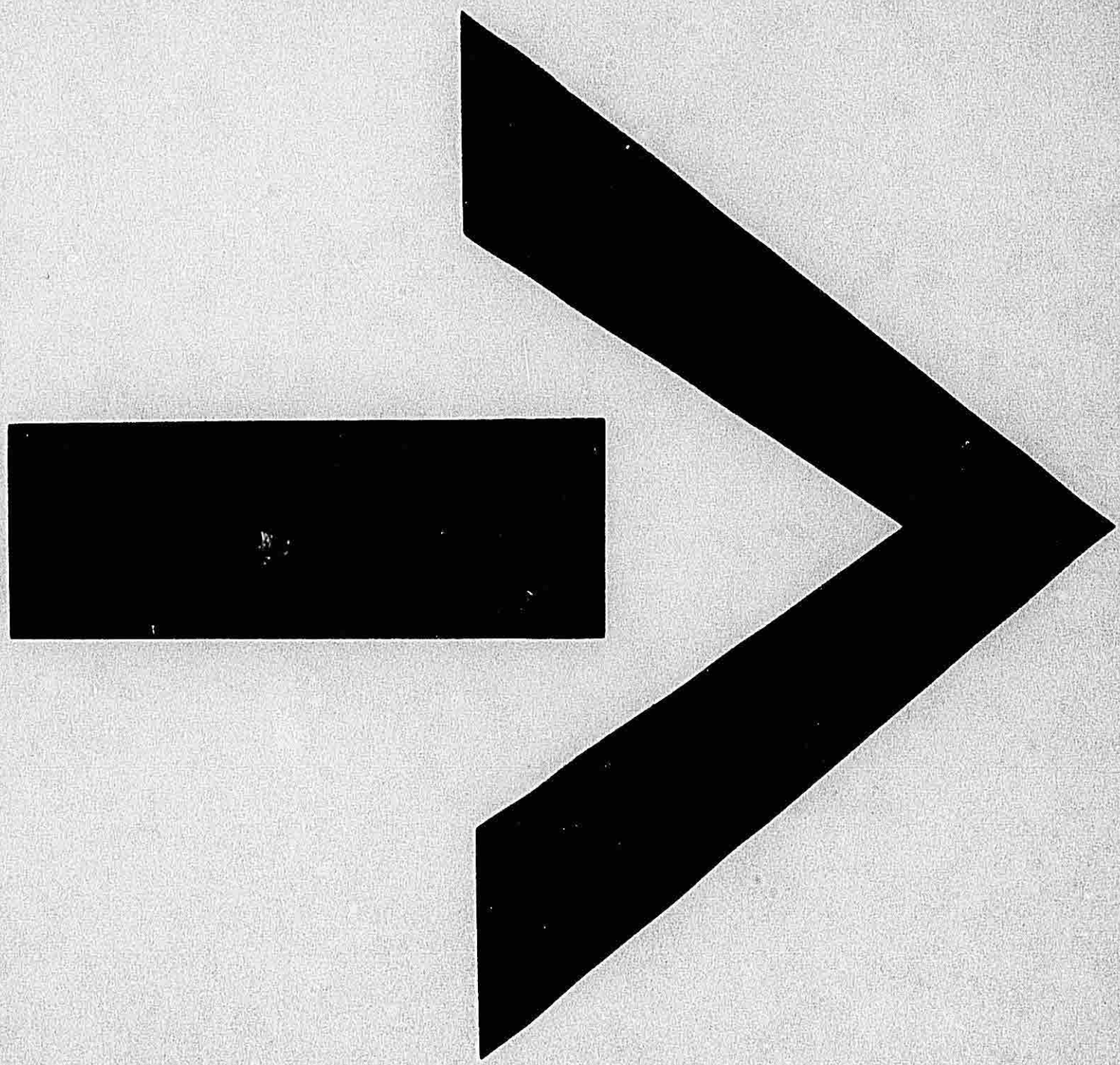
4. Each waveform is identified by a numbered diamond, which correlates with a numbered diamond found in the schematic.



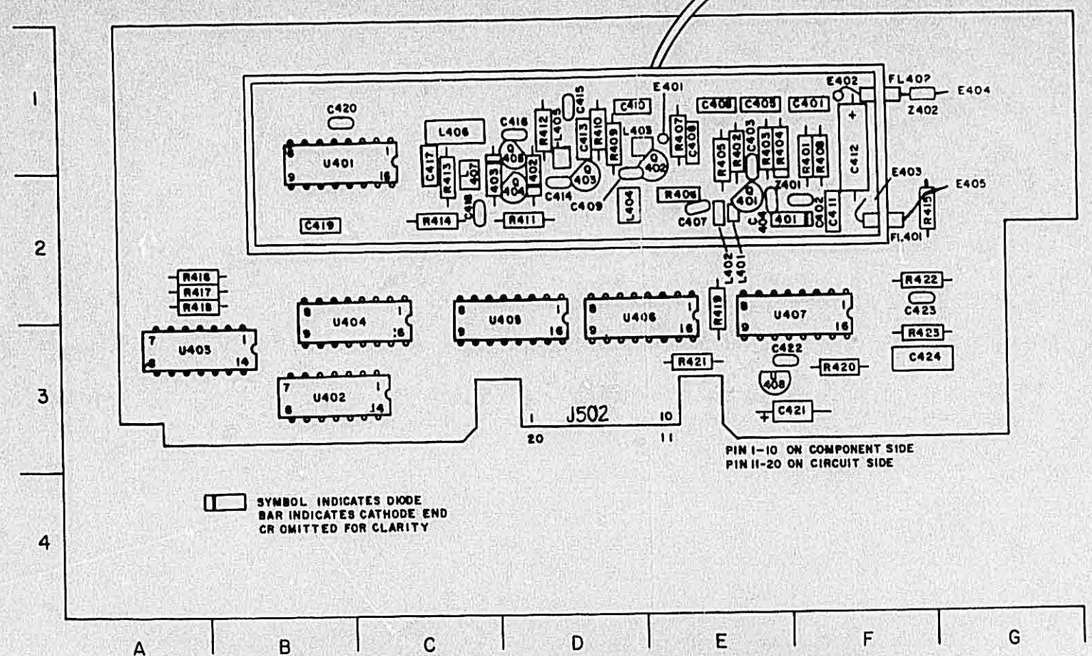
NOTES:
1. ▯ INDICATES DIODE. CR OMITTED FOR CLARITY. BAR INDICATES CATHODE END.


E
F
G
H
13.3V
11.3V
14.3V
4V
0.65V
0.72V
0.22V
0V
0V
R715 100
C712 1000
R716 1.5K
R713 1.5K
C701 1000
R705 4.7K
R710 470
L703 240µH
C734 1000
E801 +14V INPUT *
E703
C707 2.2µF 20V
Q706 SRF 215
C708 10
Q707 SRF 215
C709 47
C710 2.7
R702 470K
R706 470K
C705 2.2µF, 20V
L702 56µH
Q703 2N3391
C719 2.2µF, 20V
Q704 2N3391
Q705 2N5138
R711 330
R708 330
C733 100
E802 RECEIVER VIDEO TO P501-9,12 *
E702
R704 3.3K
R712 10
R709 1.5K
R701 68K
R717 330K
R714 330K
CR701
CR702
L701
C702 10
4
5
6
Q702 2N4124
R707 47K
C706 47
C732 100
E803 RECEIVER AGC PULSES TO P501-10,11 *
E701
R703 100K
C703 2.2µF 20V
C704 .05µF
Q701 2N3391
NO SIGNAL
-88dBM
-78dBM
-68dBM
* SEE POWER SUPPLY SCHEMATIC

B
C
D
C715
C704
SHIELD
C734
C-50033-C
D-95289-B



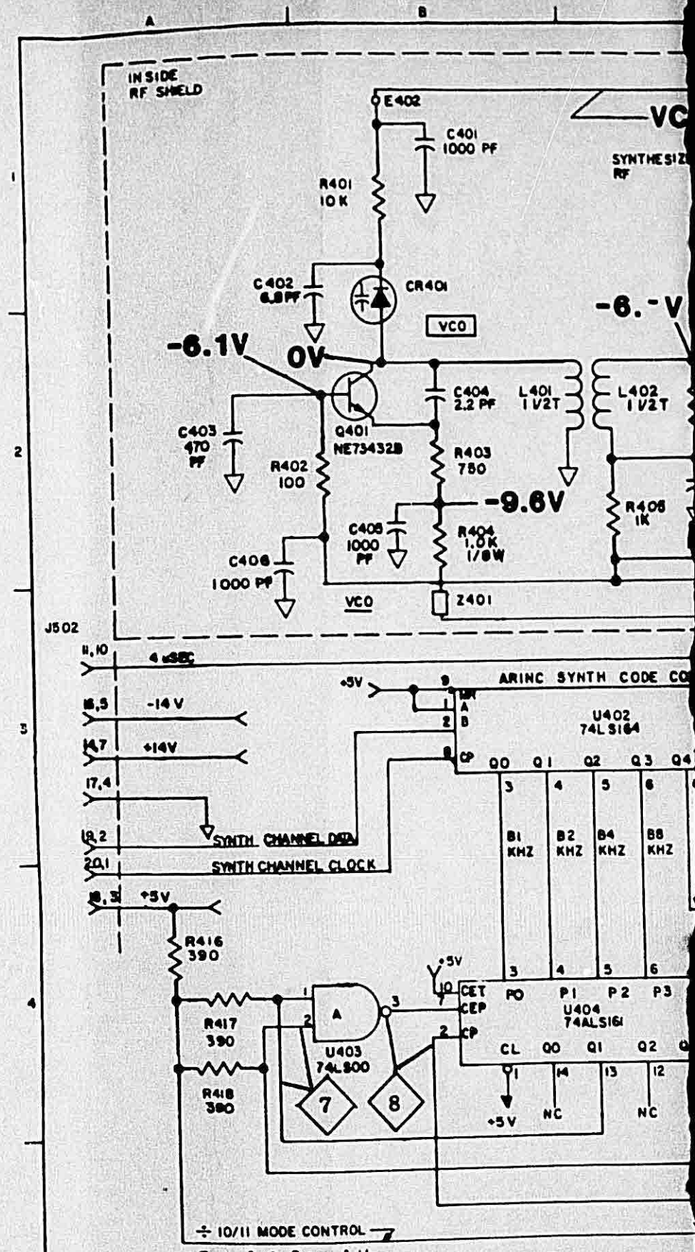
Action: O=Original, A=added, C=changed, D=deleted / Chassis Level Code / Symbol	PART NUMBER	DESCRIPTION	Grid Coordinates Schematic	Component Assy
O B C701	21291-0019	CAPACITOR, Ceramic, 1000 pF ±10%, 500 VDC	E2	F1
O B C702	24516-0100	CAPACITOR, Ceramic, NPO, 10 pF ±1 pf, 500 VDC	D2	F4
O B C703	21568-1084	CAPACITOR, Tantalum, 2.2 mF ±20%, 20 VDC	C2	F5
O B C704	24515-0007	CAPACITOR, Ceramic, .05 mF +80%, -20%, VDC	C2	E4
O B C705	21568-1084	CAPACITOR, Tantalum, 2.2 mF ±20%, 20 VDC	C2	F3
O B C706	24052-0470	CAPACITOR, Mica, 47 pF ±5%, 300 VDC	B2	G5
O B C707	21568-1084	CAPACITOR, Tantalum, 2.2 mF ±20%, 20 VDC	B2	G1
O B C708	24516-0100	CAPACITOR, Ceramic, NPO, 10 pF ±1%, 500 VDC	E1	E2
O B C709	24052-0470	CAPACITOR, Mica, 47 pF ±5%, 300 VDC	D1	E2
O B C710	24509-0279	CAPACITOR, Ceramic, 2.7 pF ±5%, 500 VDC	D1	E2
O B C711	24553-0001	CAPACITOR, Ceramic, NPO, 3.3 pF ±5%, 500 VDC	D1	D3
O B C712	21291-0019	CAPACITOR, Ceramic, 1000 pF ±10%, 500 VDC	D1	E2
O B C713	24509-0478	CAPACITOR, Ceramic, .47 pF ±5%, 500 VDC	D1	D2
O B C714	24553-0001	CAPACITOR, Ceramic, NPO, 33 pF ±5% 500 VDC	D1	D3
O B C715	21291-0019	CAPACITOR, Ceramic, 1000 pF ±10%, 500 VDC	D1	D1
O B C716	24509-0109	CAPACITOR, Ceramic, 1.0 pF ±5%, 500 VDC	C1	D2
O B C717	24509-0279	CAPACITOR, Ceramic, 2.7 pF ±5%, 500 VDC	C1	C3
O B C718	24553-0001	CAPACITOR, Ceramic, NPO, 33 pF ±5%, 500 VDC	C1	C3
O B C719	21568-1084	CAPACITOR, Tantalum, 2.2 pF ±20%, 20 VDC	C1	E2
O B C720	24509-0478	CAPACITOR, Ceramic, .47 pF ±5%, 500 VDC	C1	C3
O B C721	24553-0001	CAPACITOR, Ceramic, NPO, 33 pF ±5%, 500 VDC	B1	C3
O B C722	24509-0109	CAPACITOR, Ceramic, 1.0 pF ±5%, 500 VDC	B1	C3
O B C723	24509-0279	CAPACITOR, Ceramic, 2.7 pF ±5%, 500 VDC	B1	B3
O B C724	21291-0019	CAPACITOR, Ceramic, 1000 pF ±10%, 500 VDC	B1	C2
O B C725	24553-0001	CAPACITOR, Ceramic, NPO, 33 pF ±5%, 500 VDC	B1	B3
O B C726	24509-0478	CAPACITOR, Ceramic, .47 pF ±5%, 500 VDC	B1	B3
O B C727	24553-0001	CAPACITOR, Ceramic, NOP, 33 pF ±5%, 500 VDC	A1	B3
O B C728	21291-0019	CAPACITOR, Ceramic, 1000 pF ±10%, 500 VDC	A1	B2
O B C729	24509-0109	CAPACITOR, Ceramic, 1 pF ±5%, 500 VDC	A1	B3
O B C730	24052-0470	CAPACITOR, Mica, 47 pF ±5%, 500 VDC	A1	A3
O B C731	24052-0270	CAPACITOR, Mica, 27 pF ±5%, 500 VDC	A1	A4
O B C732	21296-0006	CAPACITOR, Ceramic, Feedthru,100 pF ±10%,250VDC	E2	H4
O B C733	21296-0006	CAPACITOR, Ceramic, Feedthru,100 pF ±10%,250VDC	E1	H2
O B C734	21290-0008	CAPACITOR, Ceramic, Feedthru,1000pf ±20%,250VDC	A2	H1
O B CR701	75063-0001	DIODE, Microwave	E2	F3
O B CR702	75063-0001	DIODE, Microwave	B2	F3
O B L701	11798-0002	COIL, Toroid	E2	F4
O B L702	11485-0034	CHOKE, 56 ull, ±10%	D2	F3
O B L703	11451-0048	CHOKE, 240 ul!	A2	H1
O B L704	11870-0002	COIL, RF	D1	D3
O B L705	11870-0002	COIL, RF	D1	D3
O B L706	11870-0002	COIL, RF	C1	C3
O B L707	11870-0002	COIL, RF	C1	C3
O B L708	11870-0002	COIL, RF	B1	B4
O B L709	11870-0002	COIL, RF	A1	B4
O B Q701	75550-0117	TRANSISTOR, Silicon, NPN, 2N3391	D2	F4
O B Q702	75561-0036	TRANSISTOR, Silicon, NPN, 2N4124	C2	F4
O B Q703	75550-0007	TRANSISTOR, Silicon, NPN, 2N3391	C2	F3
O B Q704	7555Q-0007	TRANSISTOR, Silicon, NPN, 2N3391	C2	G2
O B Q705	75506-0001	TRANSISTOR, Silicon, PNP, 2N5138	A2	G2
O B Q706	75622-0001	TRANSISTOR, Silicon, NPN, SRF 215	E1	E2
O B Q707	75622-0001	TRANSISTOR, Silicon, NPN, SRF 215	D1	E2
O B Q708	75622-G001	TRANSISTOR, Silicon, NPN, SRF 215	C1	D2
O B Q709	75622-0001	TRANSISTOR, Silicon, NPN, SRF 215	B1	B3
O B Q710	75622-0001	TRANSISTOR, Silicon, NPN, SRF 215	A1	A3
O B R701	31218-0683	RESISTOR, Carbon Film, 68K ±5%, 1/4W	D2	E3
O B R702	31218-0474	RESISTOR, Carbon Film, 470K ±5%, 1/4W	D2	F2
O B R703	31218-0104	RESISTOR, Carbon Film, 100K ±5%, 1/4W	C2	G5
O B R704	31218-0332	RESISTOR, Carbon Film, 3.3K ±5%, 1/4W	C2	G3
O B R705	31218-0472	RESISTOR, Carbon Film, 4.7K ±5%, 1/4W	C2	F2
O B R706	31218-0474	RESISTOR, Carbon Film, 470K ±5%, 1/4W	C2	F2
O B R707	31218-0473	RESISTOR, Carbon Film, 47K ±5%, 1/4W	B2	G4
O B R708	31218-0331	RESISTOR, Carbon Film, 330 ±5%, 1/4W	B2	G3
O B R709	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4W	B2	G3
O B R710	31218-0471	RESISTOR, Carbon Film, 470 ±5%, 1/4W	A2	G2
O B R711	31218-0331	RESISTOR, Carbon Film, 330 ±5%, 1/4W	B2	G2
O B R712	31218-0100	RESISTOR, Carbon Film, 10 ±5%, 1/4W	B2	G3
O B R713	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4W	E1	E2
O B R714	31218-0334	RESISTOR, Carbon Film, 330K ±5%, 1/4W	E1	E3
O B R715	31218-0101	RESISTOR, Carbon Film, 100 ±5%, 1/4W	D1	E1
O B R716	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4W	D1	E2
O B R717	31218-0334	RESISTOR, Carbon Film, 330K ±5%, 1/4W	D1	E3
O B R718	31218-0101	RESISTOR, Carbon Film, 100 ±5%, 1/4W	D1	D1
O B R719	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4W	C1	D2
O B R720	31218-0334	RESISTOR, Carbon Film, 330K ±5%, 1/4W	C1	D3
O B R721	31218-0101	RESISTOR, Carbon Film, 100 ±5%, 1/4W	B1	C1
O B R722	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4W	B1	C2
O B R723	31218-0334	RESISTOR, Carbon Film, 330K ±5%, 1/4W	B1	B3
O B R724	31218-0101	RESISTOR, Carbon Film, 100 ±5%, 1/4W	A2	B1
O B R725	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4W	A1	B2
O B R726	31218-0334	RESISTOR, Carbon Film, 330K ±5%, 1/4W	A1	A4

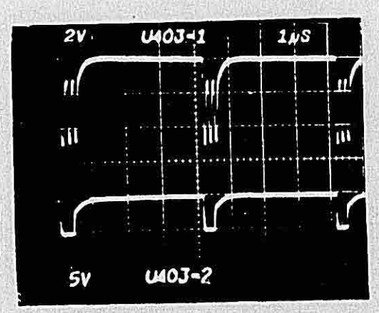


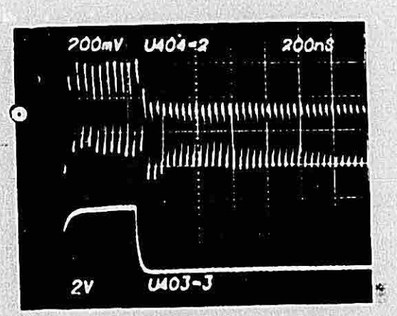
U402 ARINC TO SYNTHESIZER CODE CONVERSION

MHz	ARINC A	ARINC B	ARINC C	ARINC D	Output from U403 A8	Output from U403 A4	Output from U403 A2	Output from U403 A1	KHz	ARINC A	ARINC B	ARINC C	ARINC D	Output from U402 B8	Output from U402 B4	Output from U402 B2	Output from U402 B1
108	0	X	X	0	X	0	0	X	.0	X	0	X	X	X	0	0	X
109	0	X	X	X	X	0	0	0	.1	0	0	X	X	X	0	0	0
110	X	0	X	X	0	X	X	X	.2	0	X	0	X	0	X	X	X
111	0	0	X	X	0	X	X	0	.3	X	0	0	X	0	X	X	0
112(.0/.2)	0	X	0	X	0	X	0	X	.4	X	0	X	0	0	X	0	X
112(.3/.8)	0	X	0	X	0	X	0	0	.5	X	X	0	0	0	X	0	0
113	X	0	0	X	0	0	X	X	.6	X	X	0	X	0	0	X	X
114	X	0	X	0	0	0	X	0	.7	X	X	X	0	0	0	X	C
115	X	X	0	0	0	0	0	X	.8	0	X	X	0	0	0	0	X
116	X	X	0	X	0	0	0	0	.9	0	X	X	X	0	0	0	0
117>	X	X	X	0	X	X	X	X									

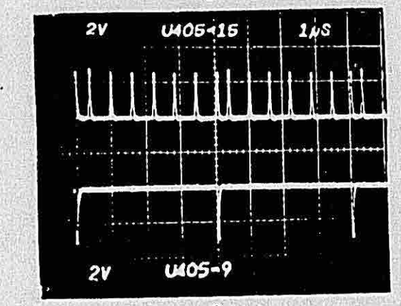
X= LOGIC HIGH 0= LOGIC LOW Dwg. No. TP00810

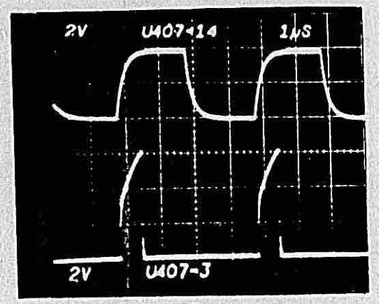






7 108.9MHz 8





9 108.9MHz 10

OSCILLOSCOPE MAIN TRIGGERING

MODE: NORM (Trigger)
COUPLING: DC
SOURCE: INTERNAL
DISPLAY MODE: ALTERNATE
PROBE COUPLING: AC

WAVEFORM NOTES

The waveform photographs provide the following information:

1. Scope Vertical Scale (volts/div).
   In the upper left corner of the photograph is displayed the volts/div for the upper trace. In the lower left corner is displayed the volts/div for the lower trace.

2. Scope Horizontal Scale (time/div)
   In the upper right corner of the photograph is displayed the time/div for BOTH the upper and bottom traces.

3. Test Points
   The top center edge of the photograph identifies the test point for the upper trace. The bottom center edge identifies the test point for the bottom trace.

4. Each waveform is identified by a numbered diamond, which correlates with a numbered diamond found in the schematic.

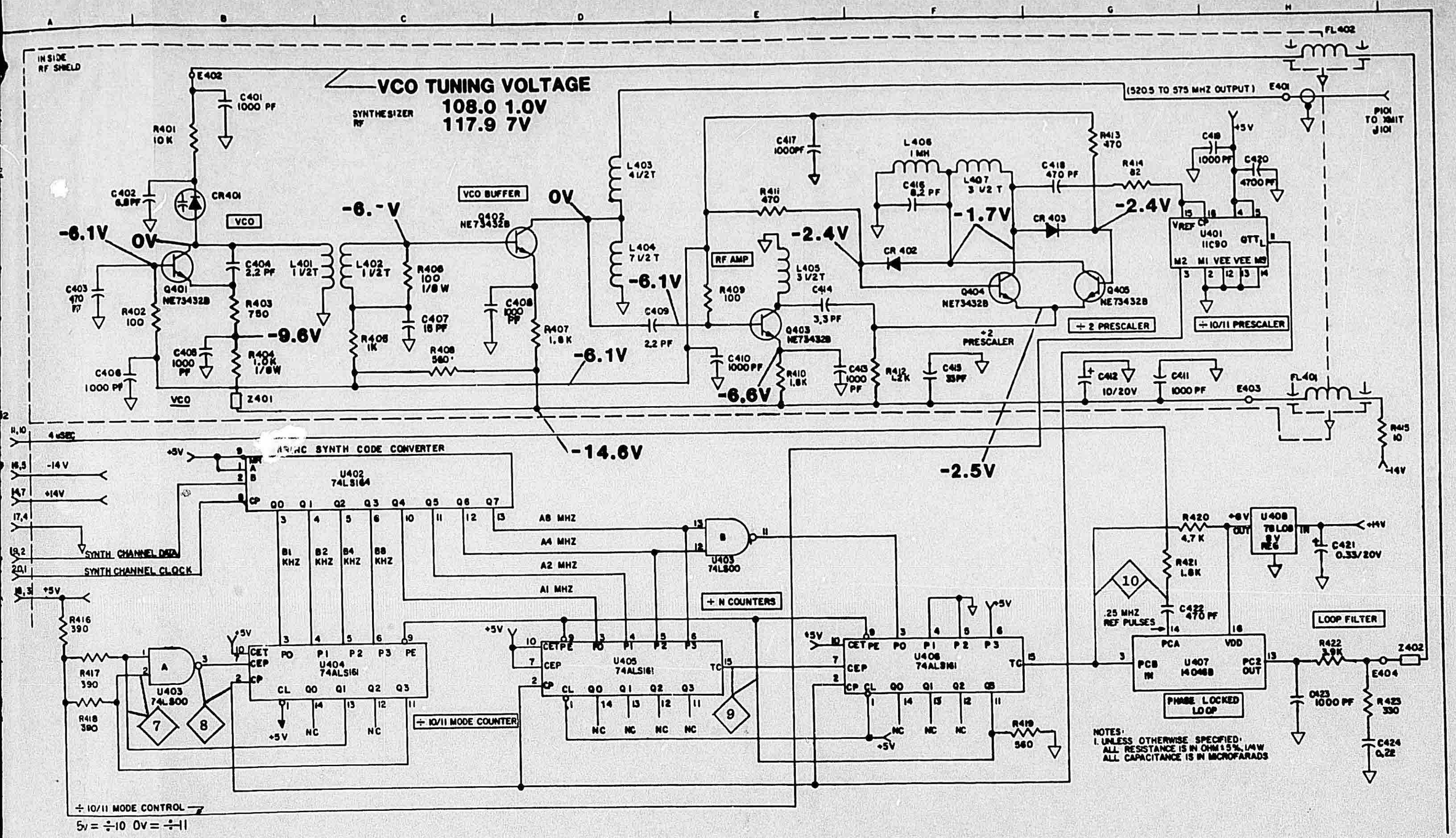
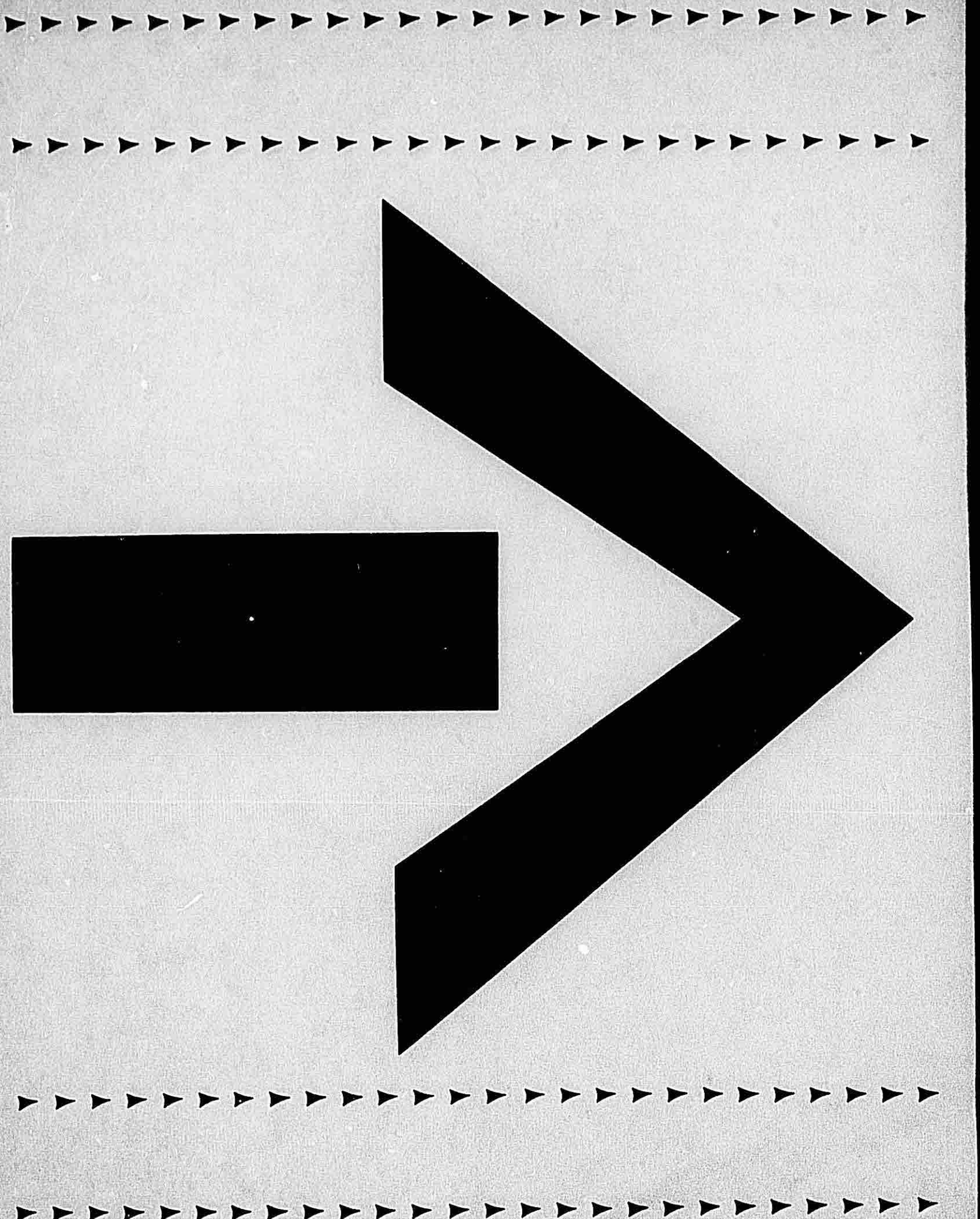
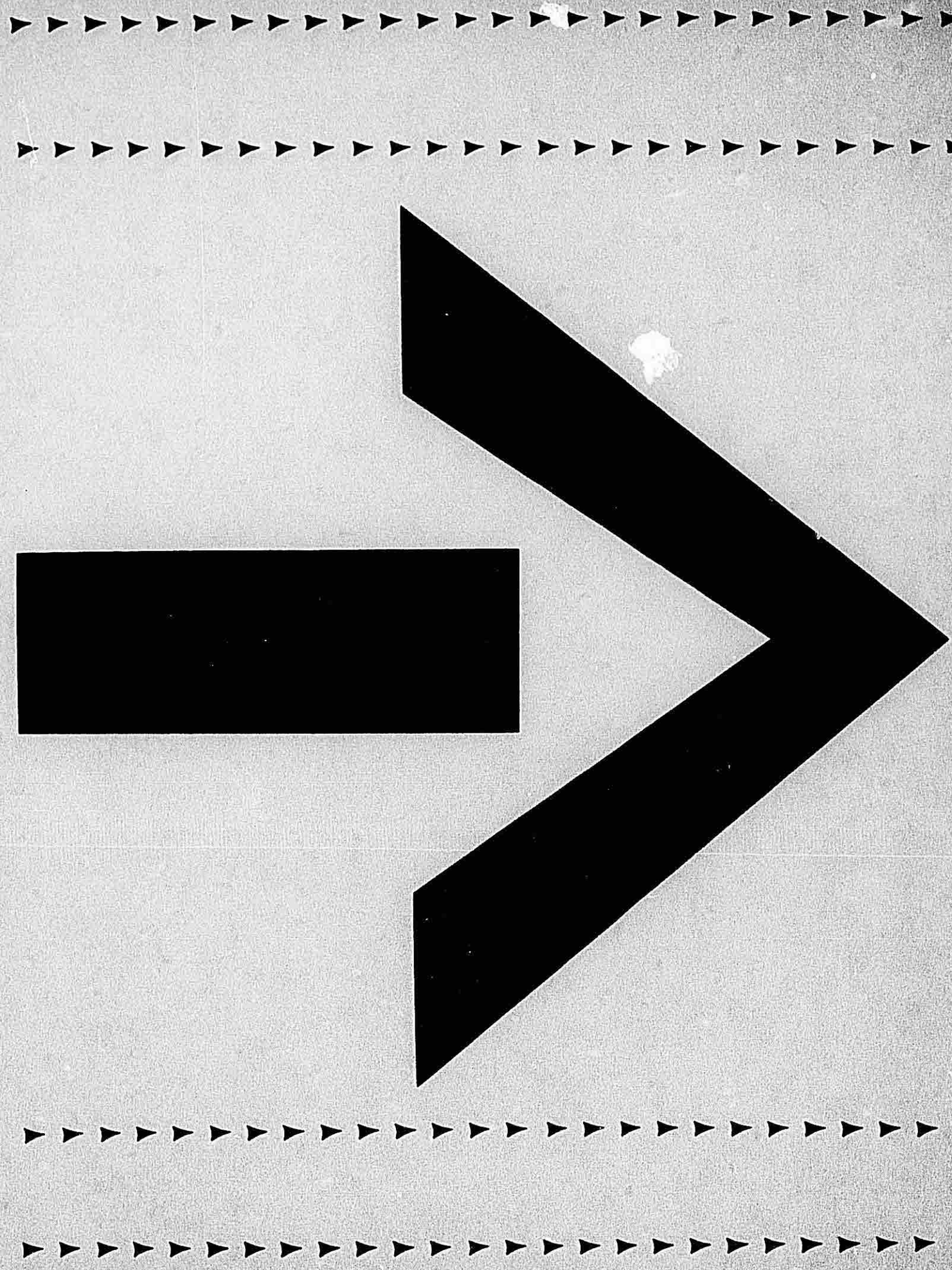


FIGURE 6-9 VCO/SYNTHESIZER SCHEMATIC



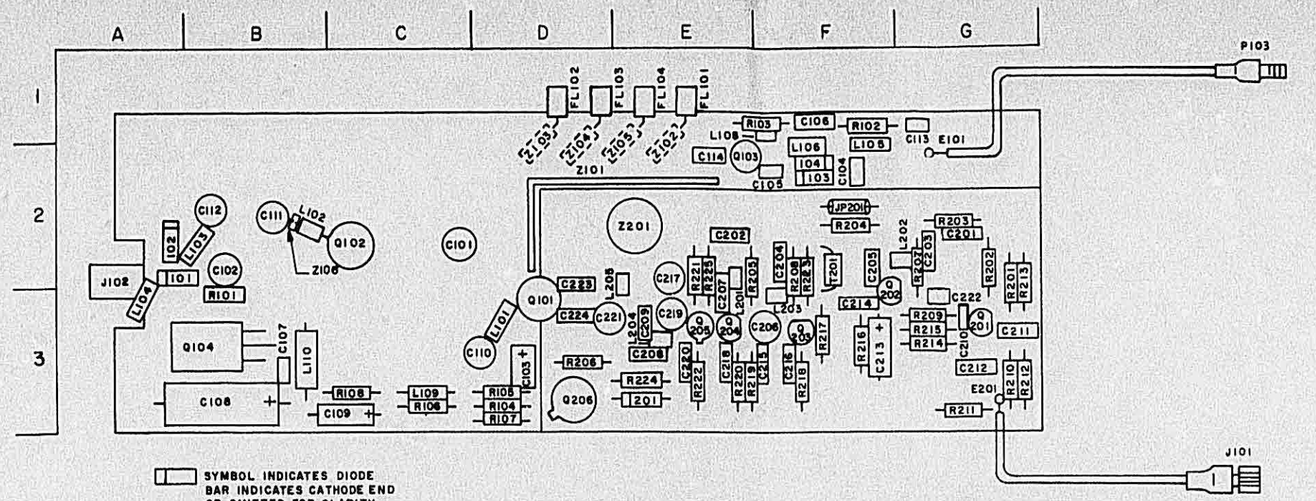


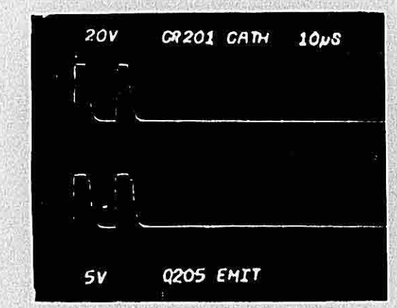
IDME 891 VCO/SYNTH BOARD ELECTRICAL PARTS LIST
BW 01426-0101

Action: Original, added, changed, deleted / Chassis Level Code / Symbol	PART NUMBER	DESCRIPTION	Grid Coordinates Schematic	Component Assy
O B C401	24562-0032	CAP., Ceramic, 1000pF, +80-20% , 63VDC	F1	B1
O B C402	24552-1689	CAP., Ceramic, 6.8pF ±.5pF, NPO, 50 VDC	F2	B1
O B C403	24551-0002	CAP., Ceramic, 470pF, ±20%, 50 VDC	E1	A2
O B C404	24552-1229	CAP., Ceramic, 2.2pF, ±.5pF, NPO, 50VDC	E2	B2
O B C405	24562-0032	CAP., Ceramic, 1000pF, +80-20%, 63VDC	E1	B2
O B C406	24562-0032	CAP., Ceramic, 1000pF, +80-20%, 63VDC	E1	A2
O B C407	24552-1150	CAP., Ceramic, 15pF, ±10%, 50 VDC	E2	C2
O B C408	24562-0032	CAP., Ceramic, 1000pF, +80-20%, 63VDC	E1	C2
O B C409	24552-1229	CAP., Ceramic, 2.2pF ±.5pF, NPO, 50VDC	D2	D2
O B C410	24562-0032	CAP., Ceramic, 1000pF, +80-20%, 63VDC	D1	E2
O B C411	24562-0032	CAP., Ceramic, 1000pF, +80-20%, 63VDC	F2	G3
O B C412	21568-1092	CAP., Tant., 10uF, ±20%, 20VDC	F1	G3
O B C413	24562-0032	CAP., Ceramic, 1000pF, +80-20%, 63VDC	D1	E2
O B C414	24552-1339	CAP., Ceramic, 3.3pF ±.5pF, NPO, 50VDC	D2	E2
O B C415	24552-1330	CAP., Ceramic, 33pF, NPO ±10%, 50VDC	D1	F2
O B C416	24552-3829	CAP., Ceramic, 8.2pF, N150 ±.5pF, 50VDC	D1	F2
O B C417	24562-0032	CAP., Ceramic, 1000pF, +80-20%, 63VDC	C1	E1
O B C418	24551-0002	CAP., Ceramic, 470pF ±20%, 50VDC	C2	G1
O B C419	24562-0032	CAP., Ceramic, 1000pF, +80-20%, 63VDC	B2	H1
O B C420	24550-0472	CAP., Ceramic, .0047uF, ±20%, 100VDC	B1	H1
O B C421	21568-1074	CAP., Tant., 0.33uF, ±20%, 20VDC	E3	H3
O B C422	24551-0002	CAP., Ceramic, 470pF, ±20%, 50VDC	E3	G4
O B C423	24551-0005	CAP., Ceramic, 1000pF, ±10%, 63VDC	F2	H4
O B C424	23113-0101	CAP., Metal Poly 0.22uF, 100VDC ±10%	F3	H5
O B CR401	75069-0001	DIODE, Silicon Tuning	F2	B1
O B CR402	75028-0001	DIODE, Silicon, Switching, 25V	D2	F2
O B CR403	75028-0001	DIODE, Silicon, Switching, 25V	C2	G2
O B FL401	24564-0001	FILTER, EMI	F2	H3
O B FL402	24564-0001	FILTER, EMI	F1	H1
O B L401	11936-0001	COIL, RF, 1-1/2 Turns	E2	B2
O B L402	11713-0008	COIL, RF, P.S. 1-1/2 Turns	E2	C2
O B L403	11713-0015	COIL, RF, P.A. 4-1/2 Turns	E1	D1
O B L404	11713-0005	COIL, RF, P.S. 7-1/2 Turns	D2	D2
O B L405	11713-0004	COIL, RF, P.S. 3-1/2 Turns	D1	E2
O B L406	11485-0040	COIL, 1MH.	C1	F1
O B L407	11713-0004	CHOKE, RF, P.S. 3-1/2 Turns	C2	F1
O B J101	41244-0002	CONNECTOR, Male	E1	H1
O B Q401	75677-0001	TRANSISTOR, Silicon, NPN, NE73432B	E2	B2
O B Q402	75677-0001	TRANSISTOR, Silicon, NPN, NE73432B	E1	D2
O B Q403	75677-0001	TRANSISTOR, Silicon, NPN, NE73432B	D2	E2
O B Q404	75677-0001	TRANSISTOR, Silicon, NPN, NE73432B	D2	F2
O B Q405	75677-0001	TRANSISTOR, Silicon, NPN, NE73432B	D1	G2
O B R401	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	F1	B1
O B R402	31218-0101	RESISTOR, Carbon, Film, 100 ±5% 1/4w	E1	B2
O B R403	31218-0751	RESISTOR, Carbon, Film, 750 ±5% 1/4w	E1	B2
O B R404	31216-0102	RESISTOR, Carbon, Film, 1K ±5% 1/8w	E1	B2
O B R405	31218-0102	RESISTOR, Carbon, Film, 1K ±5% 1/4w	E1	C2
O B R406	31216-0101	RESISTOR, Carbon, Film, 100 ±5% 1/8w	E2	C2
O B R407	31218-0182	RESISTOR, Carbon, Film, 1.8K ±5% 1/4w	E1	D2
O B R408	31218-0561	RESISTOR, Carbon, Film, 560 ±5% 1/4w	F1	C2
O B R409	31218-0101	RESISTOR, Carbon, Film, 100 ±5% 1/4w	D1	E2
O B R410	31218-0182	RESISTOR, Carbon, Film, 1.8K ±5% 1/4w	D1	E2
O B R411	31218-0471	RESISTOR, Carbon, Film, 470 ±5% 1/4w	D2	E2
O B R412	31218-0122	RESISTOR, Carbon, Film, 1.2K ±5% 1/4w	D1	F2
O B R413	31218-0471	RESISTOR, Carbon, Film, 470 ±5% 1/4w	C2	G1
O B R414	31218-0820	RESISTOR, Carbon, Film, 82 ±5% 1/4w	C2	G1
O B R415	31218-0100	RESISTOR, Carbon, Film, 10 ±5% 1/4w	F2	H3
O B R416	31218-0391	RESISTOR, Carbon, Film, 390 ±5% 1/4w	A2	A4
O B R417	31218-0391	RESISTOR, Carbon, Film, 390 ±5% 1/4w	A2	A4
O B R418	31218-0391	RESISTOR, Carbon, Film, 390 ±5% 1/4w	A2	A4
O B R419	31218-0561	RESISTOR, Carbon, Film, 560 ±5% 1/4w	E3	F4
O B R420	31218-0472	RESISTOR, Carbon, Film, 4.7K ±5% 1/4w	F3	G3
O B R421	31218-0182	RESISTOR, Carbon, Film, 1.8K ±5% 1/4w	E3	G4
O B R422	31218-0392	RESISTOR, Carbon, Film, 3.9K ±5% 1/4w	F2	H4
O B R423	31218-0331	RESISTOR, Carbon, Film, 330 ±5% 1/4w	F3	H4
O B U401	74068-0003	I.C. UHF High Speed Prescaler, 11C90	B1	H2
O B U402	74170-0001	I.C. S.IN/P Out Shift Reg. 74LS164	B3	C3
O B U403	74019-0002	I.C. Quad. 2 Input NAND Gate 74LS00	A3	
U403A			B4	
U403B			E3	
U403C		NOT USED		
U403D		NOT USED		
O B U404	74218-0001	I.C. Synch 4 Bit Binary CTR 74ALS161	B3	C4
O B U405	74218-0001	I.C. Synch 4 Bit Binary CTR 74ALS161	D3	D4
O B U406	74218-0001	I.C. Synch 4 Bit Binary CTR 74ALS161	D3	F4
O B U407	74119-0001	I.C. Phase Lock Loop, 4046B (CMOS)	E3	G4
O B U408	74109-0002	I.C. 8V Reg. 100mA 78L08	E3	H3

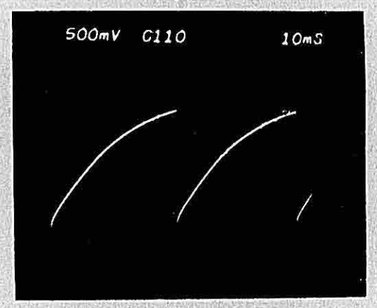
IDME 891 VCO/SYNTH BOARD ELECTRICAL PARTS LIST
BW 01426-0101

Action: Original, added, changed, deleted / Chassis Level Code / Symbol	PART NUMBER	DESCRIPTION	Grid Coordinates Schematic	Component Assy
O B Z101	11454-0003	Ferrite Bead	E2	B3
O B Z402	11454-0003	Ferrite Bead	F1	H4

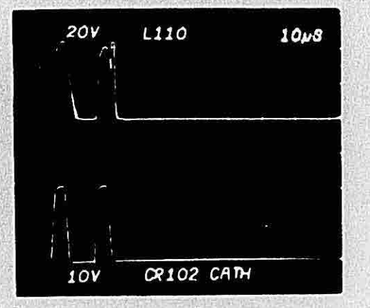




11



12



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WAVEFORM NOTES

The waveform photographs provide the following information:

1. Scope Vertical Scale (volts/div).
   In the upper left corner of the photograph is displayed the volts/div for the upper trace. In the lower left corner is displayed the volts/div for the lower trace.

2. Scope Horizontal Scale (time/div)
   In the upper right corner of the photograph is displayed the time/div for **BOTH** the upper and bottom traces.

3. Test Points
   The top center edge of the photograph identifies the test point for the upper trace. The bottom center edge identifies the test point for the bottom trace.

4. Each waveform is identified by a numbered diamond, which correlates with a numbered diamond found in the schematic.

OSCILLOSCOPE MAIN TRIGGERING

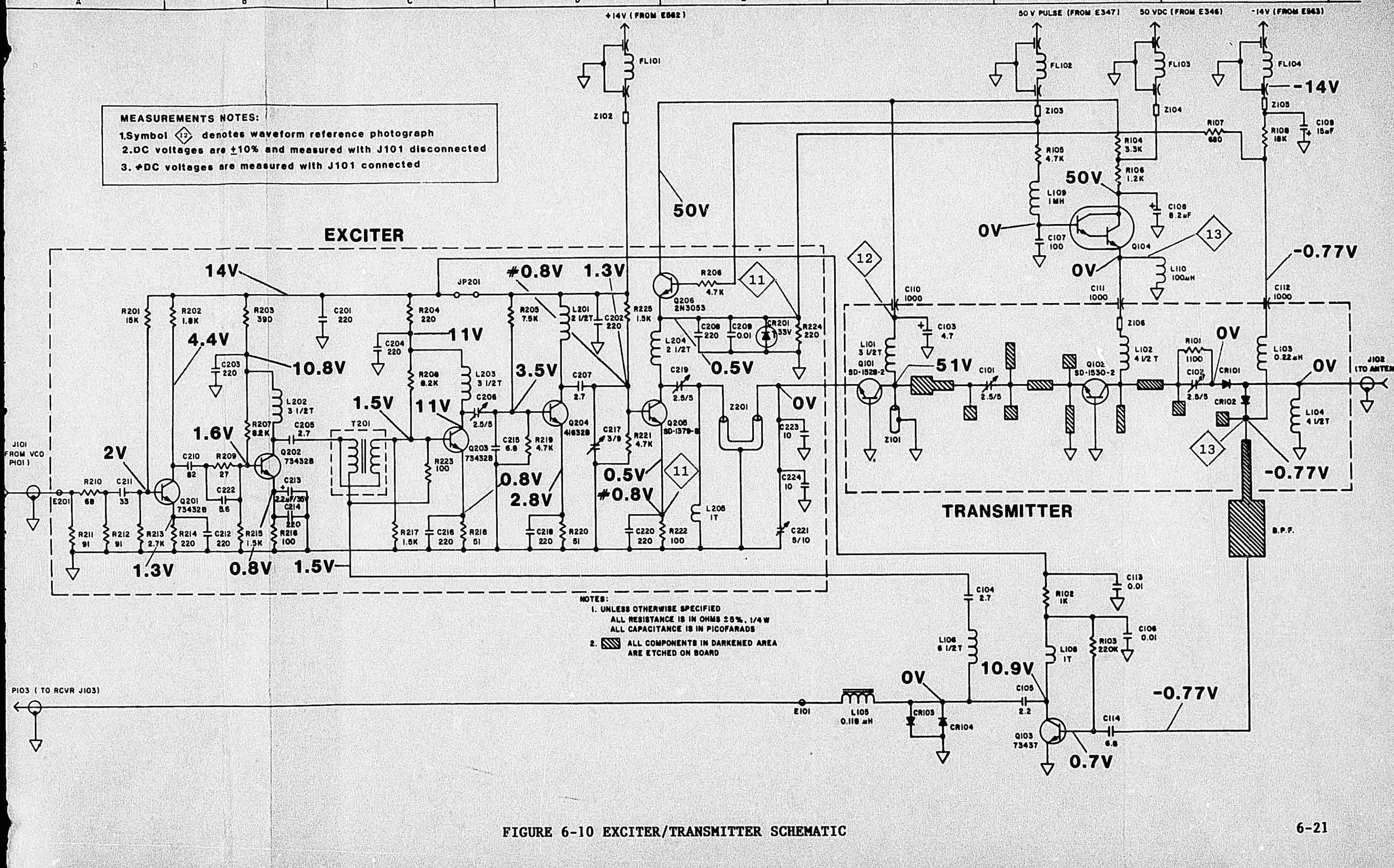
MODE: NORM (Trigger)
COUPLING: DC
SOURCE: INTERNAL
DISPLAY MODE: ALTERNATE
PROBE COUPLING: AC

MEASUREMENTS NOTES:

1. Symbol ⟨12⟩ denotes waveform reference photograph
2. DC voltages are ±10% and measured with J101 disconnected
3. ⇌DC voltages are measured with J101 connected

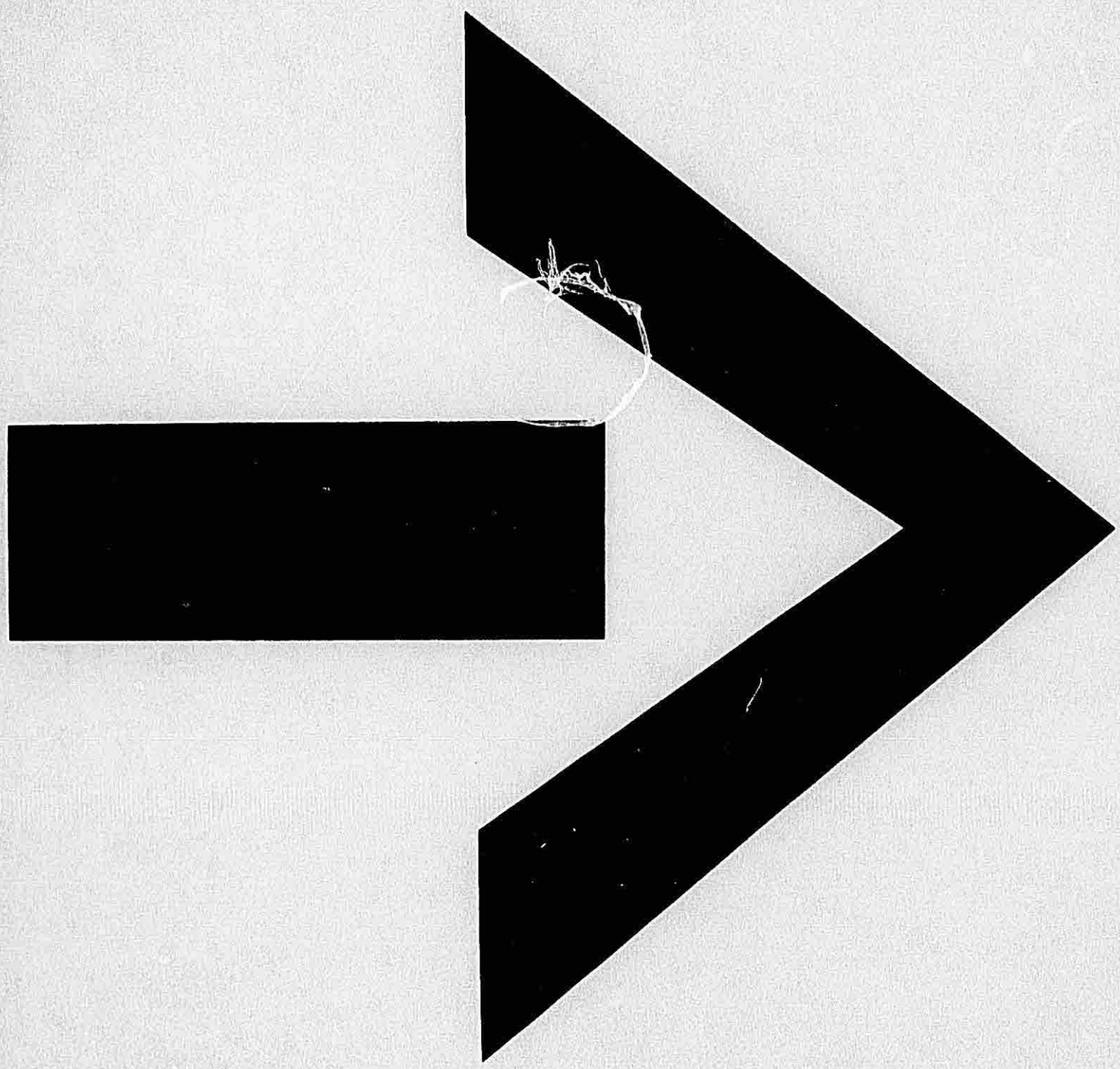
FIG

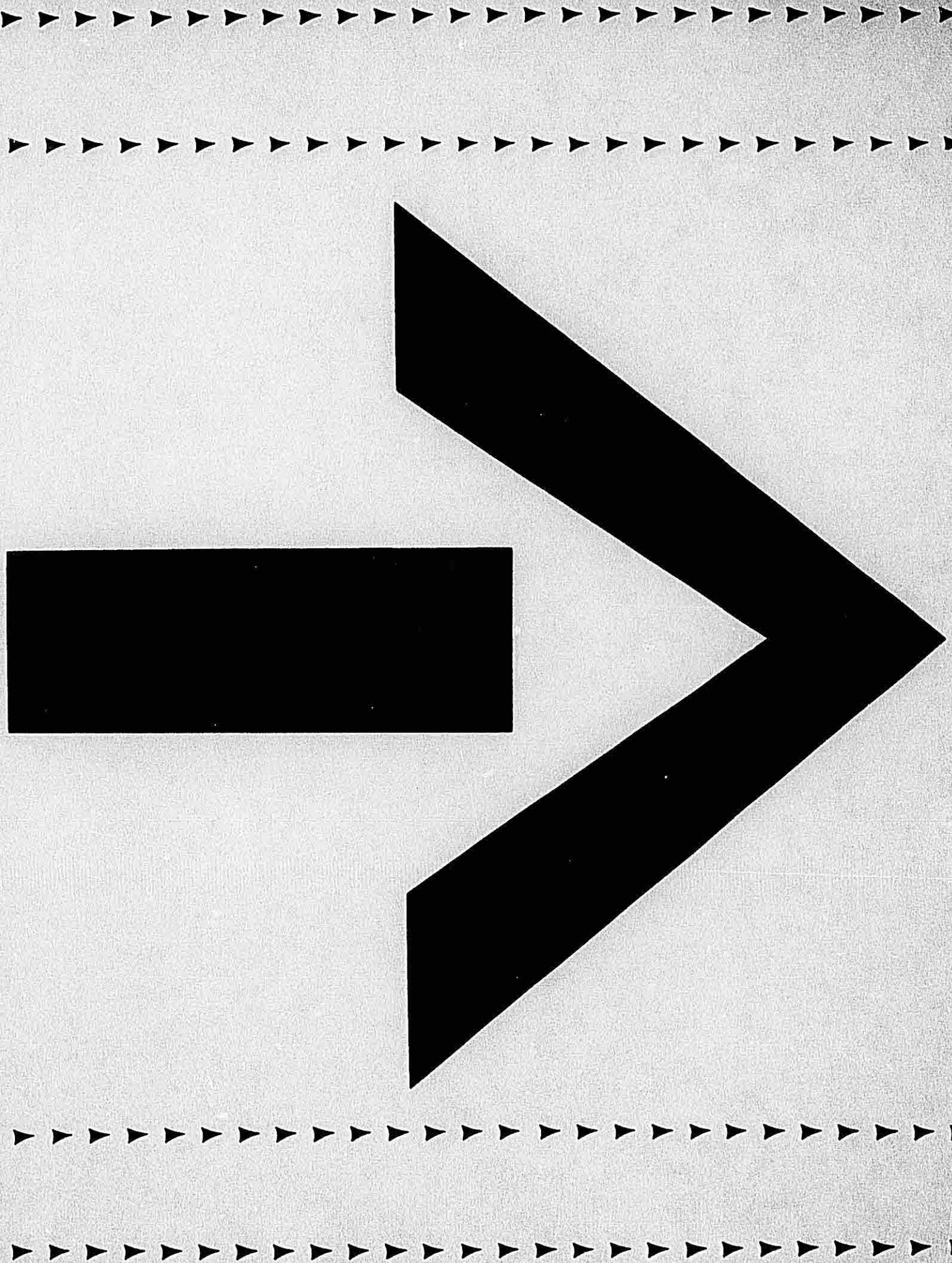
MEASUREMENTS NOTES:
1. Symbol ⟨12⟩ denotes waveform reference photograph
2. DC voltages are ±10% and measured with J101 disconnected
3. #DC voltages are measured with J101 connected



NOTES:
1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE IS IN OHMS ±5%, 1/4 W
   ALL CAPACITANCE IS IN PICOFARADS
2. ▨ ALL COMPONENTS IN DARKENED AREA ARE ETCHED ON BOARD

FIGURE 6-10 EXCITER/TRANSMITTER SCHEMATIC



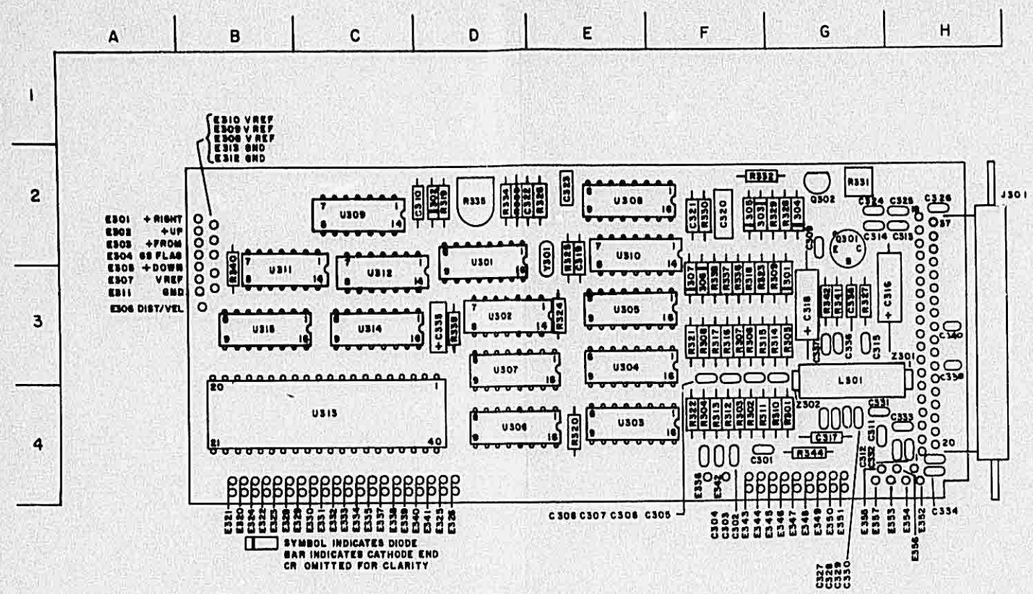


Action: Original, added, changed, deleted / Chassis Level Code / Symbol	PART NUMBER	DESCRIPTION	Grid Coordinates Schematic	Component Assy
O B C101	22053-0001	CAP, Trimmer, 2.5 - 5 pF	C2	F3
O B C102	22053-0001	CAP, Trimmer, 2.5 - 5 pF	B2	H3
O B C103	21567-0024	CAP, Electrolytic, 4.7 uF-10+75%, 100V	D3	F2
O B C104	24552-1279	CAP, Ceramic, 2.7 pF ±5%, 50V, NPO	F2	F4
O B C105	24552-1229	CAP, Ceramic, 2.2 pF ±5%, 50V, NPO	F2	G5
O B C106	24550-1103	CAP, Ceramic, .01uF ±20%, 100V	F1	G4
O B C107	24550-0101	CAP, Ceramic, 100 pF ±20%, 100V	B3	G2
O B C108	21555-0171	CAP, Tantalum, 8.2 uF ±10%, 60V	B3	G2
O B C109	21555-0028	CAP, Tantalum, 15 uF ±20%, 20V	C3	H1
O B C110	21290-0008	CAP, Feed Thru, 1000 pF ±20%, 250V	D3	F2
O B C111	21290-0008	CAP, Feed Thru, 1000 pF ±20%, 250V	B2	G2
O B C112	21290-0008	CAP, Feed Thru, 1000 pF ±20%, 250V	B2	H2
O B C113	24550-1103	CAP, Ceramic, 0.01 uF ±20%, 100V	G1	G4
O B C114	24552-1689	CAP, Ceramic, 6.8 pF ±5%, 50V, NPO	E2	G5
O B CR101	75044-0001	DIODE, Silicon Switching, Pin	A2	H3
O B CR102	75068-0001	DIODE, Silicon Switching, Pin	A2	H3
O B CR103	75063-0001	DIODE, Microwave-Schottky, ND4981-7E	F2	F5
O B CR104	75063-0001	DIODE, Microwave-Schottky, ND4981-7E	F2	F5
O B FL101	24564-0001	FILTER, EMI	E1	D1
O B FL102	24564-0001	FILTER, EMI	D1	G1
O B FL103	24564-0001	FILTER, EMI	D1	G1
O B FL104	24564-0001	FILTER, EMI	E1	H1
O B J101	41244-0001	CONNECTOR, Female		A3
O B J102	41411-0001	CONNECTOR, Female	A2	H3
O B L101	11713-0004	COIL, R.F., 3½ Turns	D3	F3
O B L102	11713-0015	COIL, R.F., 4½ Turns	B2	G3
O B L103	11485-0005	CHOKE, R.F., 0.22 uH	B2	H3
O B L104	11713-0015	COIL, R.F., 4½ Turns	A3	H3
O B L105	11935-0001	CHOKE, Toroid, 8 Turns, 0.118 uH	F2	F5
O B L106	11713-0001	COIL, R.F., 6½ Turns	F2	F4
O B L107				
O B L108	11964-0001	INDUCTOR, Hair Pin	F1	G4
O B L109	11485-0040	CHOKE, 1000 uH ±10%	C3	G2
O B L110	11451-0040	CHOKE, 100 uH ±5%	B3	G2
O B P103	41244-0002	CONNECTOR, Male		A5
O B Q101	75681-0001	TRANSISTOR, SSM SD 1528-2	D3	F3
O B Q102	75682-0001	TRANSISTOR, SSM SD 1530-2	C2	G3
O B Q103	75679-0001	TRANSISTOR, NEC 73437	E2	G5
O B Q104	75638-0007	TRANSISTOR, Silicon, Darlington, NPN	B3	G2
O B R101	31218-0112	RESISTOR, Carbon Film, 1.1K ±5%, 1/4w	B3	H3
O B R102	31218-0102	RESISTOR, Carbon Film, 1K ±5%, 1/4w	F1	G4
O B R103	31218-0224	RESISTOR, Carbon Film, 220K ±5%, 1/4w	F1	G4
O B R104	31218-0332	RESISTOR, Carbon Film, 3.3K ±5%, 1/4w	D3	G1
O B R105	31218-0472	RESISTOR, Carbon Film, 4.7K ±5%, 1/4w	D3	G1
O B R106	31218-0122	RESISTOR, Carbon Film, 1.2K ±5%, 1/4w	C3	G2
O B R107	31218-0681	RESISTOR, Carbon Film, 680 ±5%, 1/4w	D3	H1
O B R108	31218-0182	RESISTOR, Carbon Film, 1.8K ±5%, 1/4w	C3	H1
O B Z101	90119-0008	COAX, Formed Assembly	D2	F3
O B Z102	11454-0009	FERRITE BEAD	E1	D1
O B Z103	11454-0009	FERRITE BEAD	D1	G1
O B Z104	11454-0009	FERRITE BEAD	D1	G1
O B Z105	11454-0009	FERRITE BEAD	E1	H1
O B Z106	11454-0003	FERRITE BEAD	B2	G2
O B C201	24562-0024	CAP, Trapezoid, 220 pF	G2	B2
O B C202	24562-0024	CAP, Trapezoid, 220 pF	E2	D2
O B C203	24562-0024	CAP, Trapezoid, 220 pF	G2	B3
O B C204	24562-0024	CAP, Trapezoid, 220 pF	F2	C2
O B C205	24562-0001	CAP, Trapezoid, 2.7 pF	F2	B3
O B C206	22053-0001	CAP, Trimmer, 2.5 - 5 pF	F3	C3
O B C207	24562-0001	CAP, Trapezoid, 2.7 pF	E3	D3
O B C208	24562-0024	CAP, Trapezoid, 220 pF	E3	E2
O B C209	24550-0103	CAP, Ceramic, 0.01 uF ±20%, 100V	E3	E2
O B C210	24562-0019	CAP, Trapezoid, 82 pF	G3	B3
O B C211	24562-0014	CAP, Trapezoid, 33 pF	G3	A3
O B C212	24562-0024	CAP, Trapezoid, 220 pF	G3	B4
O B C213	21555-0024	CAP, Tantalum, 2.2 uF ±20%, 20V	F3	B3
O B C214	24562-0024	CAP, Trapezoid, 220 pF	F3	B3
O B C215	24562-0006	CAP, Trapezoid, 6.8 pF	F3	D3
O B C216	24562-0024	CAP, Trapezoid, 220 pF	F3	C4
O B C217	24563-0002	CAP, Trimmer, 3 - 9 pF	E2	D3
O B C218	24562-0024	CAP, Trapezoid, 220 pF	E3	D4
O B C219	22053-0001	CAP, Trimmer, 2.5 - 5 pF	E3	E3
O B C220	24562-0024	CAP, Trapezoid, 220 pF	E3	D4
O B C221	22053-0003	CAP, Trimmer, 5 - 10 pF	D3	F4
O B C222	24552-1569	CAP, Ceramic, 5.6 pF ±10%, 50V	G3	B3

IDME 891 TRANSMITTER/EXCITER ELECTRICAL PARTS LIST
BM 01423-0101

Action: Original, added, changed, deleted / Chassis Level Code / Symbol	PART NUMBER	DESCRIPTION	Grid Coordinates Schematic	Component Assy
O B C223	24562-0008	CAP, Trapezoid, 10 pF	D3	E3
O B C224	24562-0008	CAP, Trapezoid, 10 pF	D3	E3
O B CR201	75047-0005	DIODE, Zener, 33V	E3	E2
O B JP201	90123-0001	WIRE JUMPER	F2	C2
O B L201	11713-0020	COIL, R.F., 2½ Turns	E2	D2
O B L202	11713-0004	COIL, R.F., 3½ Turns	G2	B3
O B L203	11713-0004	COIL, R.F., 3½ Turns	F3	C3
O B L204	11713-0020	COIL, R.F., 2½ Turns	E3	D2
O B L205	11964-0001	INDUCTOR, Hairpin	E2	E3
O B Q201	75677-0001	TRANSISTOR, NEC 73432B	G3	A3
O B Q202	75677-0001	TRANSISTOR, NEC 73432B	F3	B3
O B Q203	75677-0001	TRANSISTOR, NEC 73432P	F3	C3
O B Q204	75678-0001	TRANSISTOR, NEC 41632B	E3	D3
O B Q205	75680-0001	TRANSISTOR, SSM SD 1379-8	E3	D3
O B Q206	75536-0003	TRANSISTOR, 2N3053	D3	E2
O B R201	31218-0153	RESISTOR, Carbon Film, 15K ±5%, 1/4w	G3	A2
O B R202	31218-0182	RESISTOR, Carbon Film, 1.8K ±5%, 1/4w	G2	B2
O B R203	31218-0391	RESISTOR, Carbon Film, 390 ±5%, 1/4w	G2	B2
O B R204	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	F2	C2
O B R205	31218-0752	RESISTOR, Carbon Film, 7.5K ±5%, 1/4w	E2	D2
O B R206	31218-0472	RESISTOR, Carbon Film, 4.7K ±5%, 1/4w	D3	E2
O B R207	31218-0822	RESISTOR, Carbon Film, 8.2K ±5%, 1/4w	G2	B3
O B R208	31218-0822	RESISTOR, Carbon Film, 8.2K ±5%, 1/4w	F2	C3
O B R209	31218-0270	RESISTOR, Carbon Film, 27 ±5%, 1/4w	G3	B3
O B R210	31218-0680	RESISTOR, Carbon Film, 68 ±5%, 1/4w	G3	A3
O B R211	31218-0910	RESISTOR, Carbon Film, 91 ±5%, 1/4w	G3	A4
O B R212	31218-0910	RESISTOR, Carbon Film, 91 ±5%, 1/4w	G3	A4
O B R213	31218-0272	RESISTOR, Carbon Film, 2.7K ±5%, 1/4w	G3	A4
O B R214	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	G3	B4
O B R215	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4w	G3	B4
O B R216	31218-0101	RESISTOR, Carbon Film, 100 ±5%, 1/4w	F3	B4
O B R217	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4w	F3	C4
O B R218	31218-0510	RESISTOR, Carbon Film, 51 ±5%, 1/4w	F3	C4
O B R219	31218-0472	RESISTOR, Carbon Film, 4.7K ±5%, 1/4w	E3	D3
O B R220	31218-0510	RESISTOR, Carbon Film, 51 ±5%, 1/4w	E3	D4
O B R221	31218-0472	RESISTOR, CARBON Film, 4.7K ±5%, 1/4w	E2	D3
O B R222	31218-0101	RESISTOR, Carbon Film, 100 ±5%, 1/4w	E3	D4
O B R223	31218-0101	RESISTOR, Carbon Film, 100 ±5%, 1/4w	F2	C3
O B R224	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	E3	E2
O B R225	31218-0152	RESISTOR, Carbon Film, 1.5K ±5%, 1/4w	E2	D2
O B T201	11962-0001	TRANSFORMER, Power Divider	F2	C3
O B Z201	90119-0009	COAX, Formed Assembly	E3	E3

SCHEMATICS SECTION 6



RANGE BOARD COMPONENT ASSY.

OSCILLOSCOPE MAIN TRIGGERING

MODE: NORM (Trigger)
COUPLING: DC
SOURCE: INTERNAL
DISPLAY MODE: ALTERNATE
PROBE COUPLING: AC

WAVEFORM NOTES

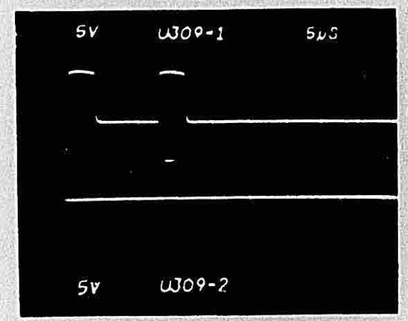
The waveform photographs provide the following information:

1. Scope Vertical Scale (volts/div).
   In the upper left corner of the photograph is displayed the volts/div for the upper trace. In the lower left corner is displayed the volts/div for the lower trace.

2. Scope Horizontal Scale (time/div)
   In the upper right corner of the photograph is displayed the time/div for **BOTH** the upper and bottom traces.

3. Test Points
   The top center edge of the photograph identifies the test point for the upper trace. The bottom center edge identifies the test point for the bottom trace.

4. Each waveform is identified by a numbered diamond, which correlates with a numbered diamond found in the schematic.



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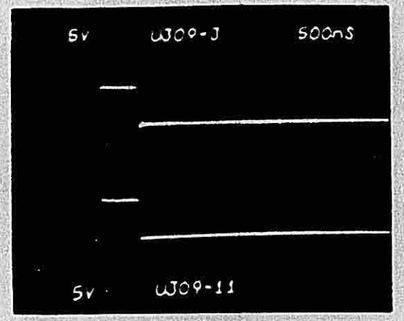

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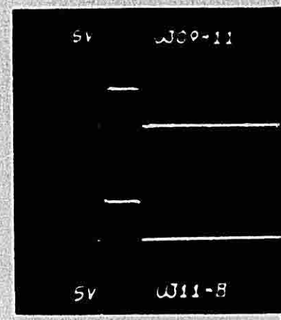

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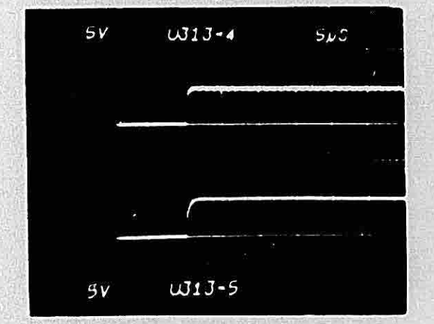

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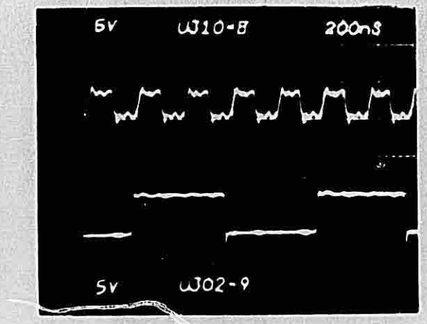

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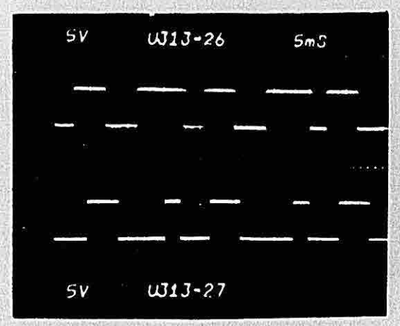

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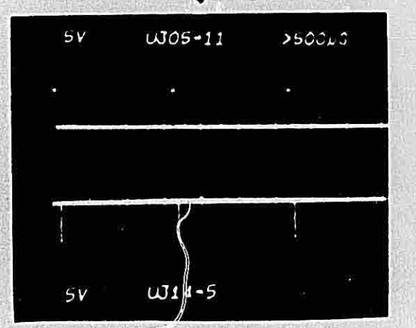

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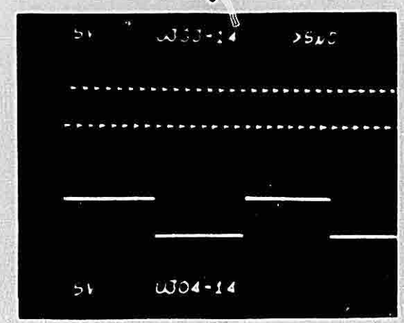

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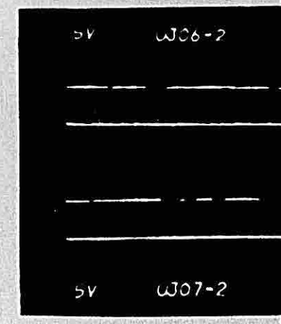

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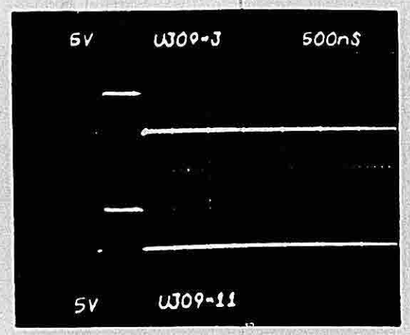

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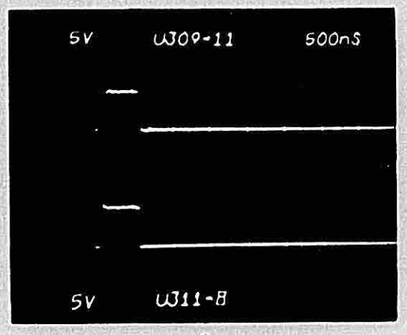

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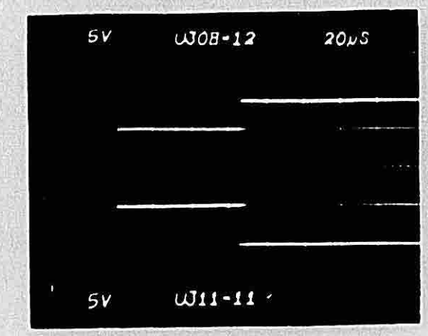

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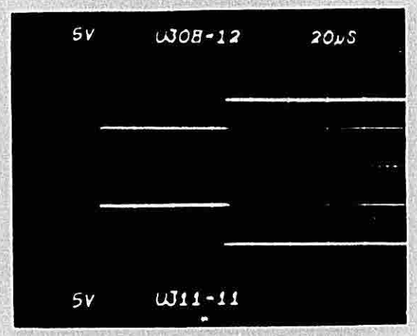

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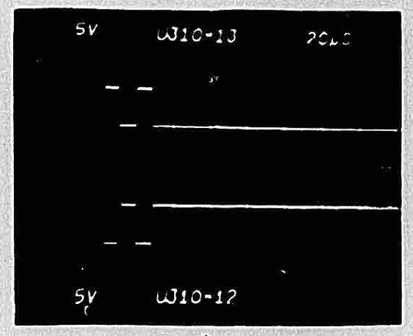

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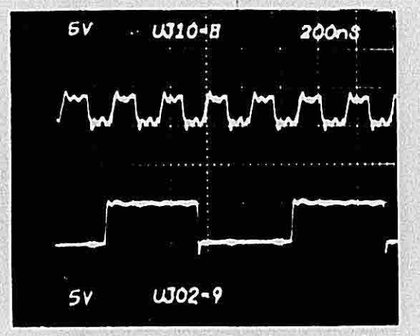

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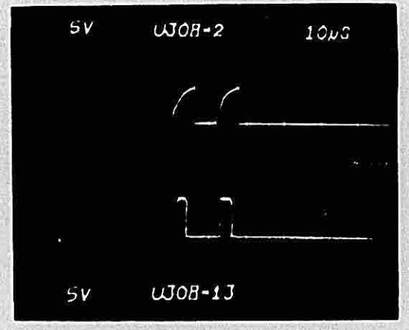

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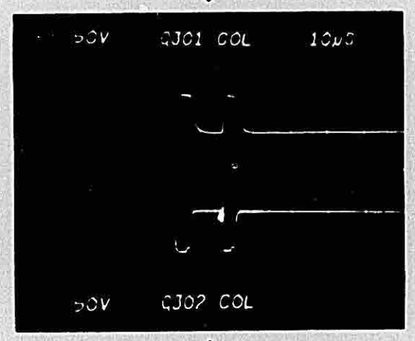

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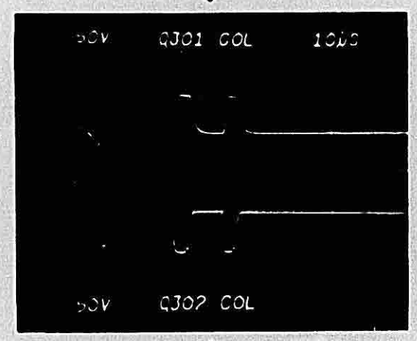

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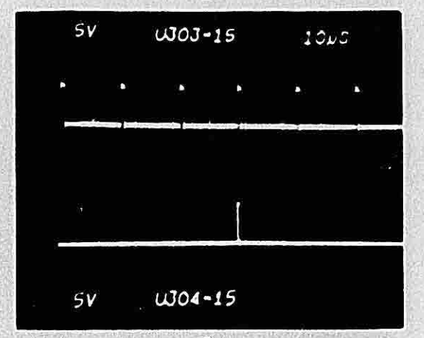

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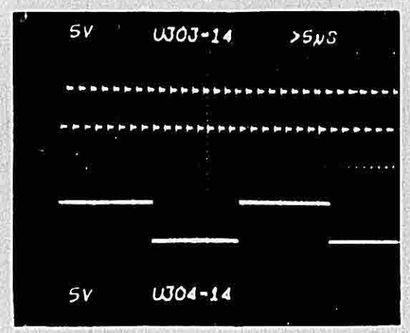

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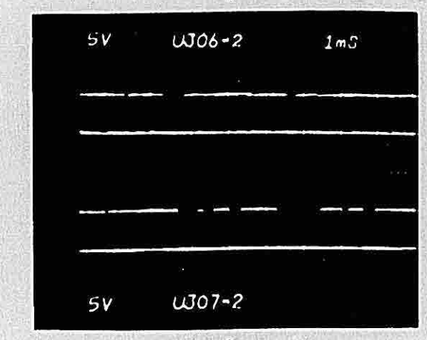

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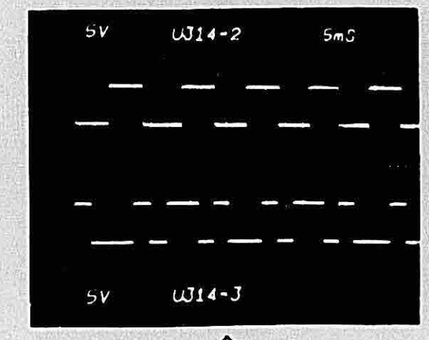

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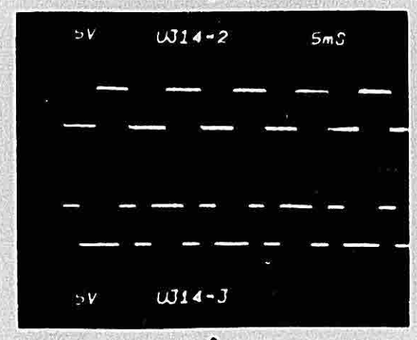

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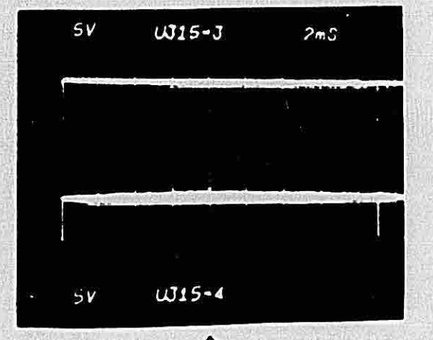
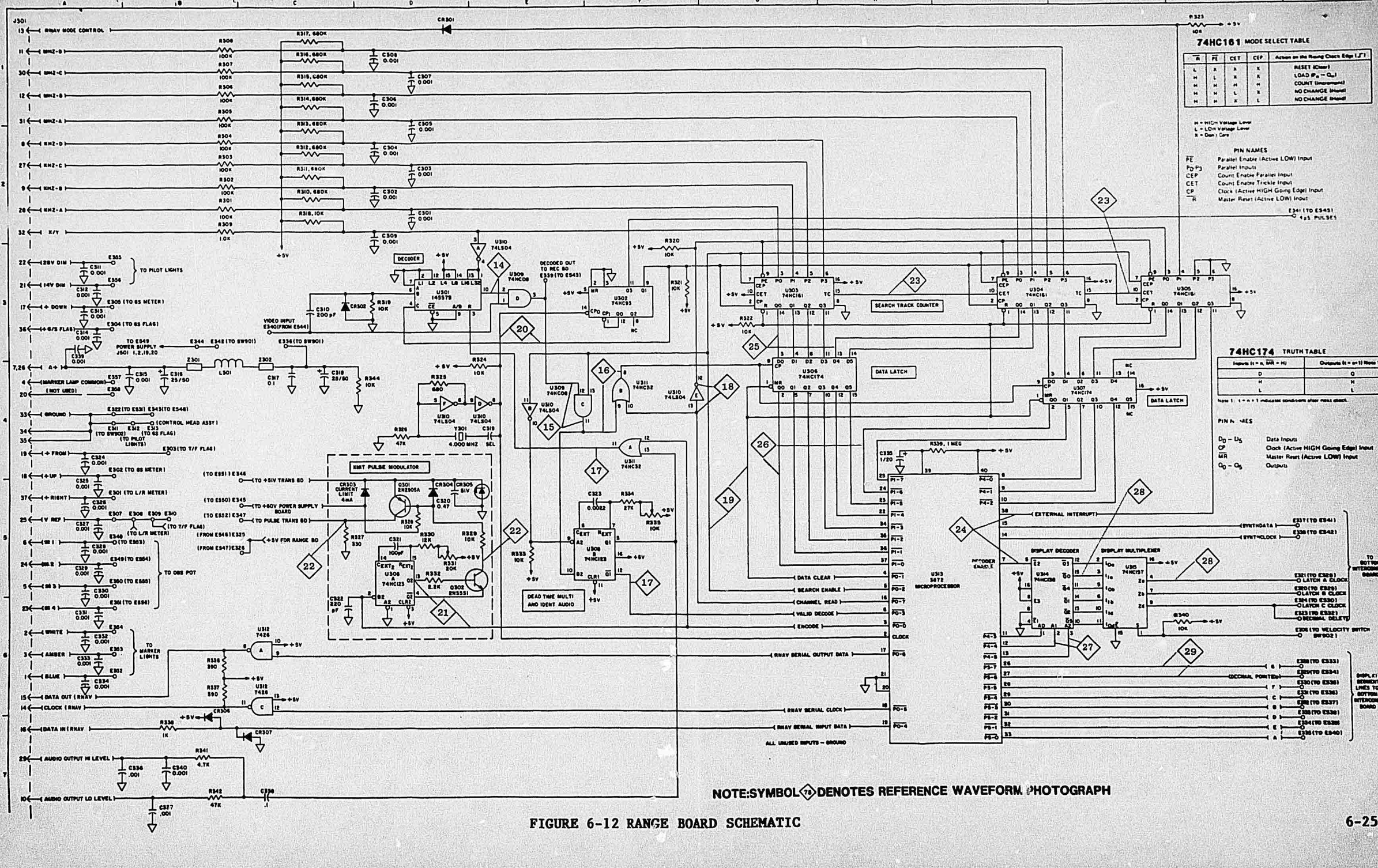


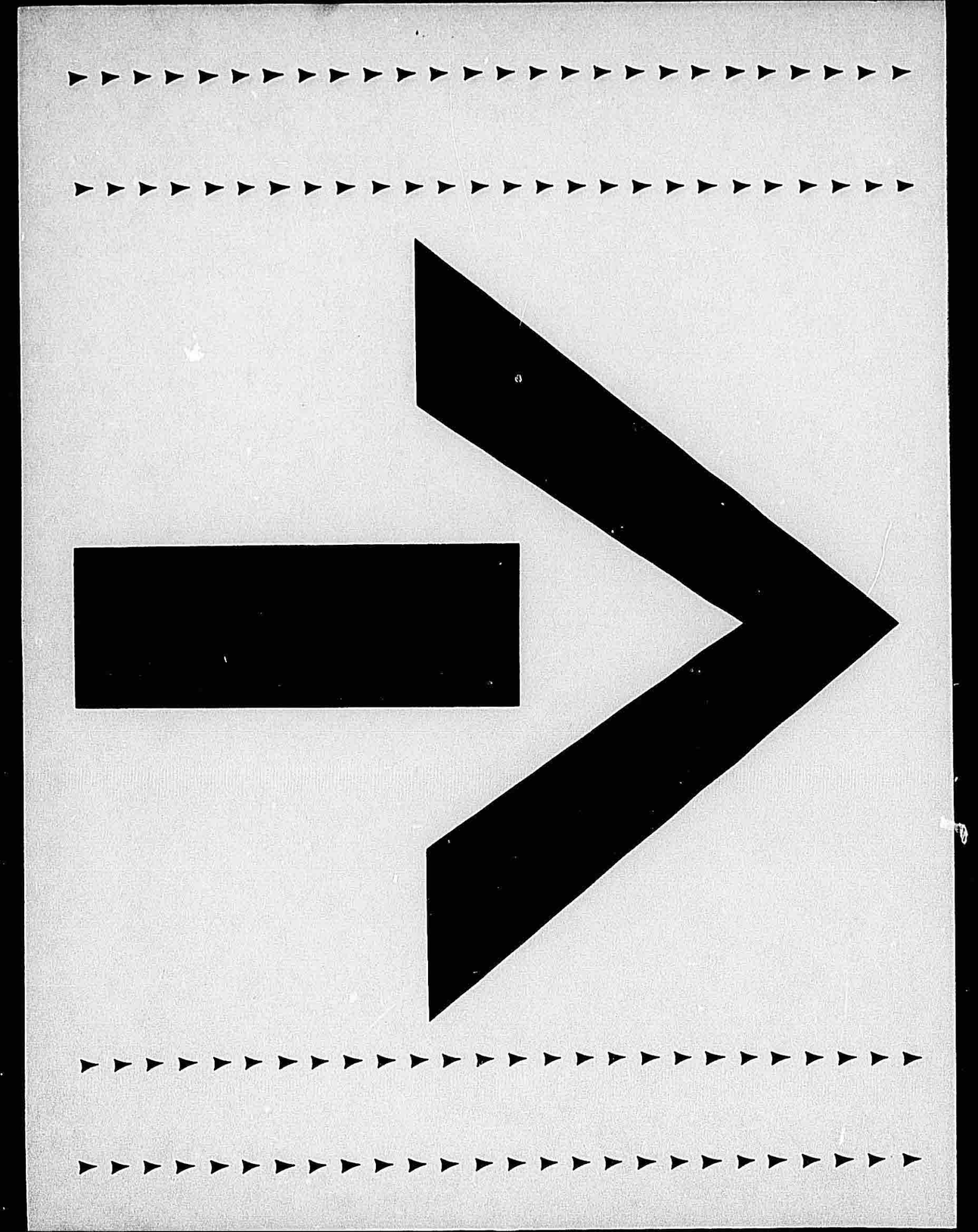
28

 FIGURE 6-11 RANGE BOARD COMPONENT ASSY. 10-83



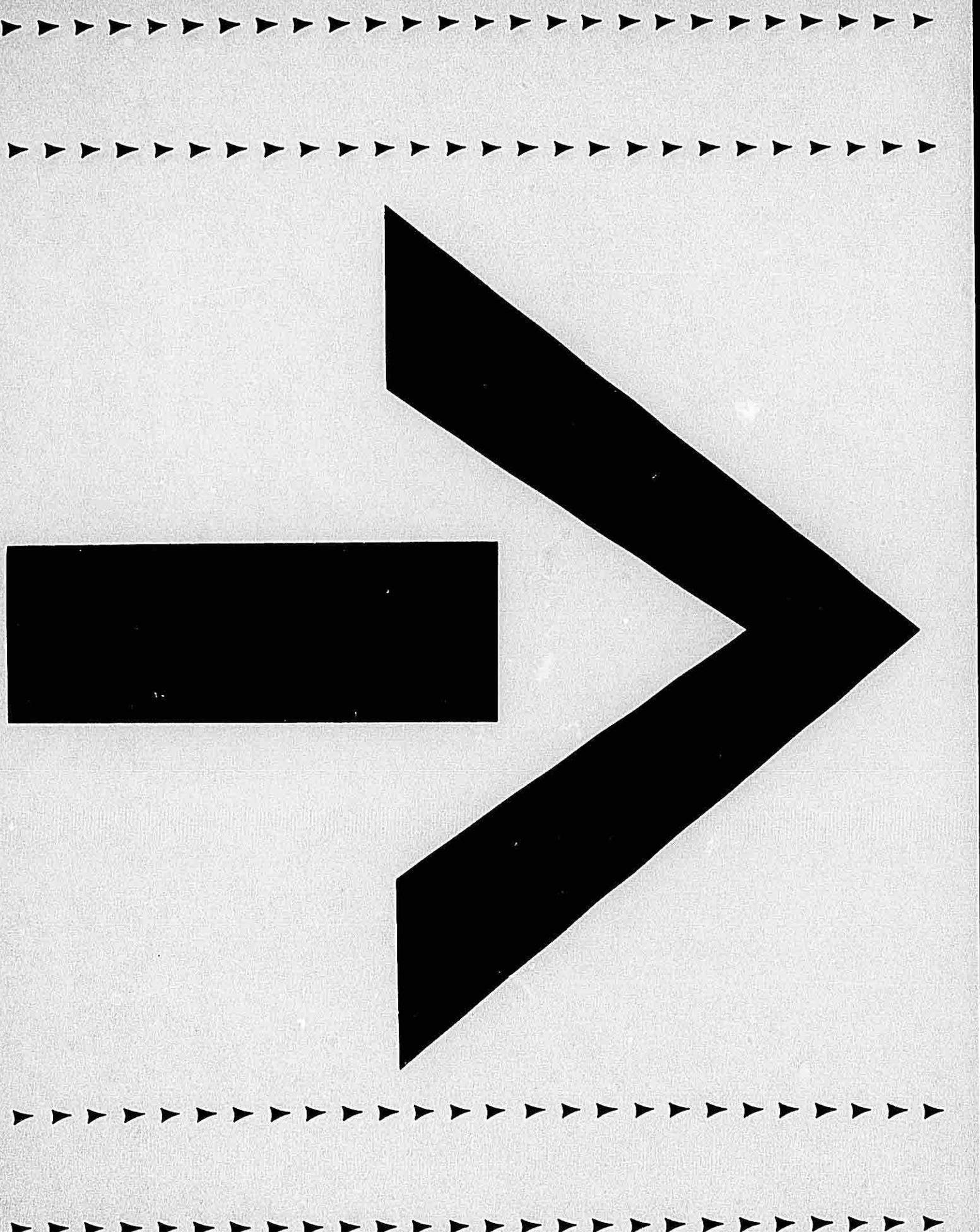
NOTE: SYMBOL ⟨78⟩ DENOTES REFERENCE WAVEFORM PHOTOGRAPH

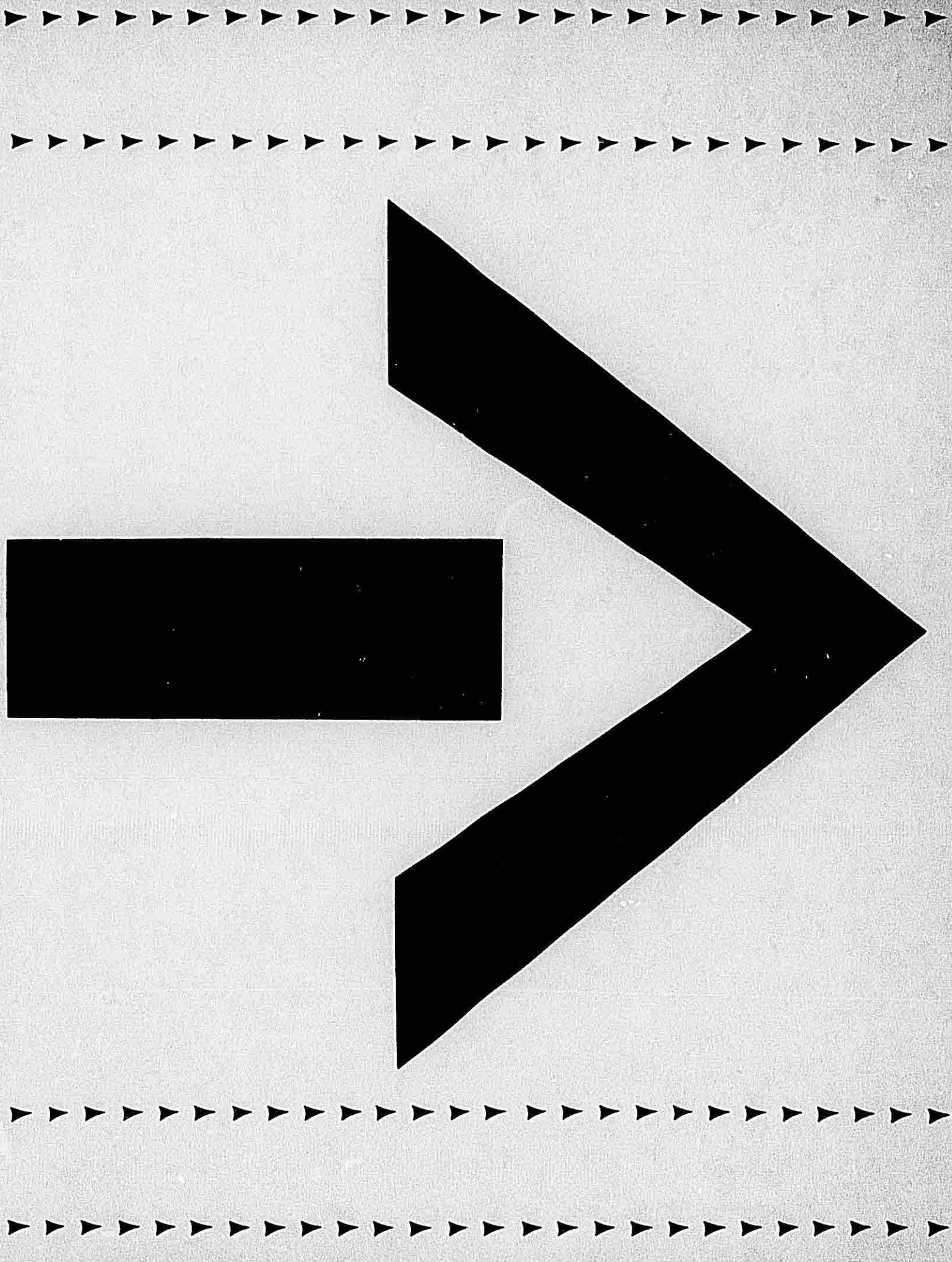
FIGURE 6-12 RANGE BOARD SCHEMATIC

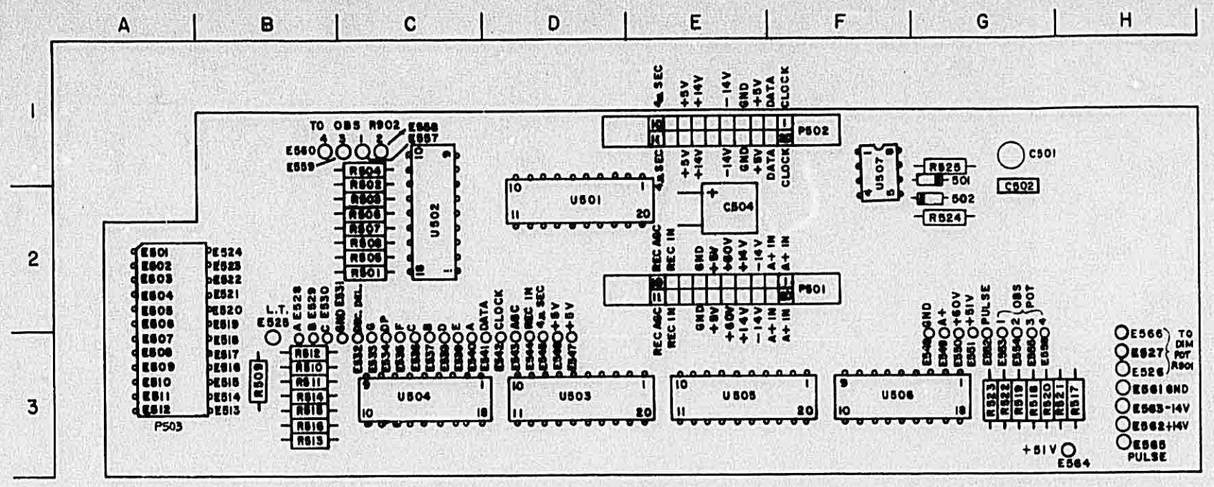


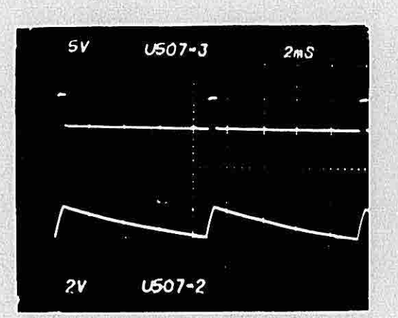
Action: Original, added, changed, deleted / Chassis Level Code / Symbol	PART NUMBER	DESCRIPTION	Grid Coordinates Schematic	Component Assy
O C C301	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	F4	D2
O C C302	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	F4	D2
O C C303	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	F4	D2
O C C304	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G3	D1
O C C305	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	F3	D1
O C C306	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	F3	D1
O C C307	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	F3	D1
O C C308	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G2	D2
O C C309	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	D2	C3
O C C310	24052-0201	CAP., Mica, 200pF ±5% 300 VDC	G4	A3
O C C311	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	H4	A3
O C C312	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	H2	A3
O C C313	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G2	A3
O C C314	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G3	B4
O C C315	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G3	B4
O C C316	21554-0006	CAP., Electrolytic, 25mF, 50VDC	G4	C4
O C C317	24565-0040	CAP., Ceramic, .1mF ±20% 100VDC	G3	C4
O C C318	21554-0006	CAP., Electrolytic, 25mF, 50VDC	E2	E4
O C C319	24052-SEL	CAP., Mica, SEL ±5% 300VDC	F2	D5
O C C320	23113-0103	CAP., Metal Poly, 0.47mF ±10% 100VDC	F2	D5
O C C321	24566-0025	CAP., Ceramic NPO, 100pF ±5% 50VDC	D2	C6
O C C322	24566-0029	CAP., Ceramic NPO, 220pF ±5% 50VDC	E2	F5
O C C323	23115-0005	CAP., Polyester, .0022uF ±5% 63VDC	G2	A4
O C C324	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	H2	A5
O C C325	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	H2	A5
O C C326	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G4	A5
O C C327	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G4	A5
O C C328	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G4	A5
O C C329	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G4	A5
O C C330	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G4	A6
O C C331	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	H4	A6
O C C332	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	H4	A6
O C C333	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	H4	A6
O C C334	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	D3	H4
O C C335	21568-1080	CAP., Tant., 1uF, 20VDC	G3	A7
O C C336	24551-0005	CAP., Ceramic, .001uF ±10% 100VDC	G3	B7
O C C337	24551-0005	CAP., Ceramic, .001uF ±10% 100VDC	G3	C7
O C C338	24567-1064	CAP., Ceramic, 0.1uF +80 -20% 100VDC	H3	A4
O C C339	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	H3	A7
O C C340	24551-0005	CAP., Ceramic, .001mF ±10% 100VDC	G3	D1
O C CR301	75028-0001	DIODE, Silicon, Switching 25V	D2	C3
O C CR302	75028-0001	DIODE, Silicon, Switching 25V	F2	D5
O C CR303	75046-0001	DIODE, Silicon, Current Limit 4mA	G2	D5
O C CR304	75028-0001	DIODE, Silicon, Switching 25V	F2	E5
O C CR305	75047-0007	DIODE, Zener, 51V, 1%	F3	B7
O C CR306	75028-0001	DIODE, Silicon, Switching 25V	F3	C7
O C CR307	75028-0001	DIODE, Silicon, Switching 25V	G3	B4
O C L301	11487-0002	CHOKE, Filter	H3	A1
O C J301	41355-0007	CONNECTOR, Jack	G2	D5
O C Q301	75634-0001	TRANSISTOR, Silicon, PNP, 2N2905A	G2	D5
O C Q302	75675-0001	TRANSISTOR, Silicon, NPN, 2N5551, 140V	G4	B2
O C R301	31218-0104	RESISTOR, Carbon, Film, 100K ±5% 1/4w	F4	B2
O C R302	31218-0104	RESISTOR, Carbon, Film, 100K ±5% 1/4w	F4	B2
O C R303	31218-0104	RESISTOR, Carbon, Film, 100K ±5% 1/4w	F4	B2
O C R304	31218-0104	RESISTOR, Carbon, Film, 100K ±5% 1/4w	G3	B1
O C R305	31218-0104	RESISTOR, Carbon, Film, 100K ±5% 1/4w	F3	B1
O C R306	31218-0104	RESISTOR, Carbon, Film, 100K ±5% 1/4w	F3	B1
O C R307	31218-0104	RESISTOR, Carbon, Film, 100K ±5% 1/4w	F3	B1
O C R308	31218-0104	RESISTOR, Carbon, Film, 100K ±5% 1/4w	G3	B2
O C R309	31218-0102	RESISTOR, Carbon, Film, 1.0K ±5% 1/4w	G4	C2
O C R310	31218-0684	RESISTOR, Carbon, Film, 680K ±5% 1/4w	F4	C2
O C R311	31218-0684	RESISTOR, Carbon, Film, 680K ±5% 1/4w	F4	C2
O C R312	31218-0684	RESISTOR, Carbon, Film, 680K ±5% 1/4w	F4	C2
O C R313	31218-0684	RESISTOR, Carbon, Film, 680K ±5% 1/4w	G3	C1
O C R314	31218-0684	RESISTOR, Carbon, Film, 680K ±5% 1/4w	F3	C1
O C R315	31218-0684	RESISTOR, Carbon, Film, 680K ±5% 1/4w	F3	C1
O C R316	31218-0684	RESISTOR, Carbon, Film, 680K ±5% 1/4w	F3	C1
O C R317	31218-0684	RESISTOR, Carbon, Film, 680K ±5% 1/4w	F3	C2
O C R318	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	D2	D3
O C R319	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	E4	F3
O C R320	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	F3	F3
O C R321	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	F4	G3
O C R322	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	F3	K1
O C R323	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	E3	E4

Action: Original, added, changed, deleted / Chassis Level Code / Symbol	PART NUMBER	DESCRIPTION	Grid Coordinates Schematic	Component Assy
O C R324	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	E2	D4
O C R325	31218-0681	RESISTOR, Carbon, Film, 680 ±5% 1/4w	E2	D4
O C R326	31218-0473	RESISTOR, Carbon, Film, 47K ±5% 1/4w	G3	C5
O C R327	31218-0331	RESISTOR, Carbon, Film, 330 ±5% 1/4w	G2	D5
O C R328	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	G2	D5
O C R329	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	F2	D5
O C R330	31218-0123	RESISTOR, Carbon, Film, 12K ±5% 1/4w	G2	D5
O C R331	32075-0009	RESISTOR, Variable Cermet, 20K	F2	D5
O C R332	31218-0222	RESISTOR, Carbon, Film, 2.2K ±5% 1/4w	D2	E5
O C R333	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	D2	F5
O C R334	31218-0273	RESISTOR, Carbon, Film, 27K ±5% 1/4w	D2	F5
O C R335	32075-0004	RESISTOR, Variable Cermet, 10K	F3	B6
O C R336	31218-0391	RESISTOR, Carbon, Film, 390 ±5% 1/4w	F3	B6
O C R337	31218-0391	RESISTOR, Carbon, Film, 390 ±5% 1/4w	F3	B7
O C R338	31218-0102	RESISTOR, Carbon, Film, 1K ±5% 1/4w	D3	I4
O C R339	31218-0105	RESISTOR, Carbon, Film, 1 Meg ±5% 1/4w	B3	K6
O C R340	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	G3	B7
O C R341	31218-0472	RESISTOR, Carbon, Film, 4.7K ±5% 1/4w	G3	B7
O C R342	31218-0473	RESISTOR, Carbon, Film, 47K ±5% 1/4w	G4	D4
O C R343		NOT USED		
O C R344	31218-0103	RESISTOR, Carbon, Film, 10K ±5% 1/4w	D2	D3
O C U301	74217-0001	I.C., 1/64 Bit Var. Length S/R 14557B (CMOS)	D3	F3
O C U302	74248-0093	I.C., 4 Bit Binary Cntr 74HC93 (LST^{2}L)	E4	G3
O C U303	74248-0161	I.C., Synch. 4 Bit Binary Cntr. 74HC161	E3	I3
O C U304	74248-0161	I.C., Synch. 4 Bit Binary Cntr. 74HC161	E3	K3
O C U305	74248-0161	I.C., Synch. 4 Bit Binary Cntr. 74HC161	D4	G4
O C U306	74248-0174	I.C., Hex D-Flip-Flop 74HC174	D3	J4
O C U307	74248-0174	I.C., Hex D-Flip-Flop 74HC174	E2	
O C U308	74248-0123	I.C., Dual S.S. Multi 74HC123		D5
U308A				F5
U308B			C2	
O C U309	74248-0008	I.C., Quad 2 Input AND Gate 74HC08		
U309A				
U309B				E4
U309C				E3
U309D			E2	
O C U310	74051-0003	I.C., Hex Inverter 74LS04		E3
U310A				E4
U310B				
U310C				E4
U310D				F4
U310E				D4
U310F			B3	
O C U311	74248-0032	I.C., Quad 2 Input OR Gate 74HC32		F4
U311A				F4
U311B				
U311C				
U311D			C3	
O C U312	74234-0001	I.C., Quad 2 Input NAND Gate H.V.7426		C6
U312A				
U312B				C6
U312C				
U312D			C4	H5
O C U313	74214-0002	I.C., Microprocessor, 3872	C3	I5
O C U314	74248-0138	I.C., 8 Bit Multiplex/Demultiplex 74HC138	B3	J5
O C U315	74248-0157	I.C., Quad 2 Input Multiplexer 74HC157		
O C Y301	72064-0001	Crystal, Quartz, 4.000MHz	E2	D4
O C Z301	11454-0003	Ferrite Bead	H3	B4
O C Z302	11454-0003	Ferrite Bead	G3	C4









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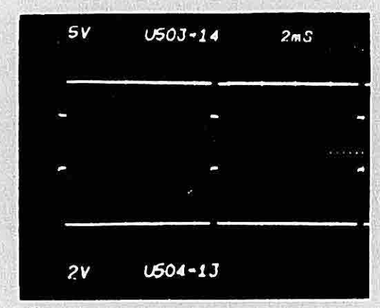

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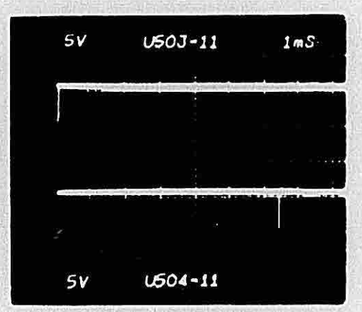

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DIMMER SET TO MAXIMUM BRIGHTNESS

WAVEFORM NOTES

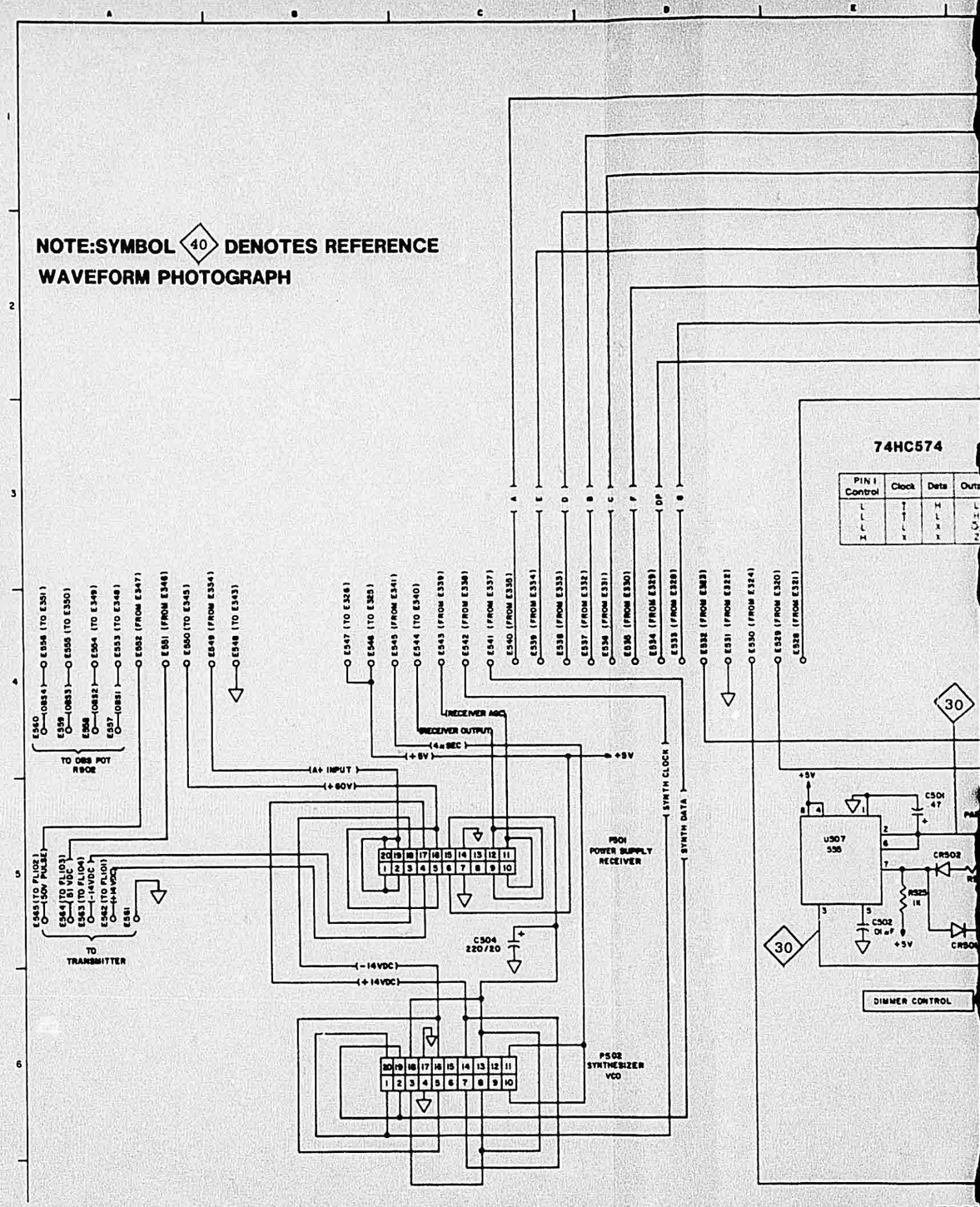
The waveform photographs provide the following information:

1. Scope Vertical Scale (volts/div).
   In the upper left corner of the photograph is displayed the volts/div for the upper trace. In the lower left corner is displayed the volts/div for the lower trace.
2. Scope Horizontal Scale (time/div)
   In the upper right corner of the photograph is displayed the time/div for **BOTH** the upper and bottom traces.
3. Test Points
   The top center edge of the photograph identifies the test point for the upper trace. The bottom center edge identifies the test point for the bottom trace.
4. Each waveform is identified by a numbered diamond, which correlates with a numbered diamond found in the schematic.

OSCILLOSCOPE MAIN TRIGGERING

MODE: NORM (Trigger)
COUPLING: DC
SOURCE: INTERNAL
DISPLAY MODE: ALTERNATE
PROBE COUPLING: AC

NOTE:SYMBOL ◇40 DENOTES REFERENCE WAVEFORM PHOTOGRAPH



FIGU

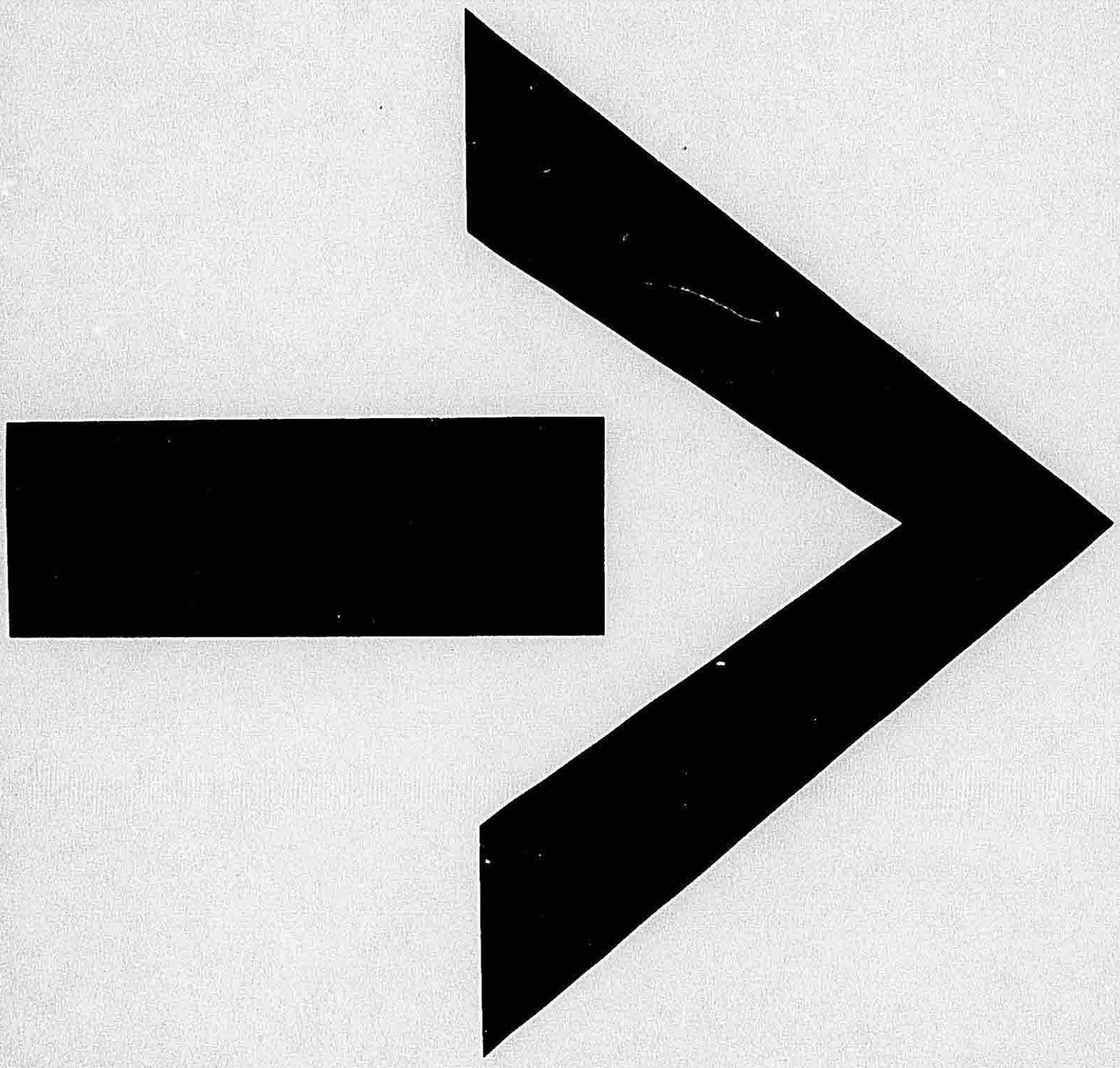
74HC574

PIN 1 Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established

DIMMER CONTROL

FIGURE 6-13 BOTTOM INTERCONNECT BOARD SCHEMATIC



IDNE 891 BOTTON INTERCONNECT BOARD ELECTRICAL PARTS LIST
BM-014301-0101

Action: Original, added, changed, deleted
Chassis Level Code
Symbol
Grid Coordinates
Schematic
Component Assy

	PART NUMBER	DESCRIPTION		
O C P503	90755-0001	RIBBON CABLE, Assembly	A2	K1
O C C501	21564-0157	CAP, Tantalum, .47uF ±10%, 35V	G1	E5
O C C502	23115-0113	CAP, Polyester, 0.01 uF ±10%, 63V	G2	E5
O C C504	21567-0037	CAP, Electrolytic, 220uF ±20%, 25V	E2	C5
O C CR501	75028-0001	DIODE, Silicon Switching	G2	E5
O C CR502	75028-0001	DIODE, Silicon Switching	G2	E5
O C P501	41362-0104	CONNECTOR, Receptable PWR Supply	E2	C5
O C P502	41362-0104	CONNECTOR, Receptable VCO	E1	C6
O C R501	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	C2	J1
O C R502	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	C2	J1
O C R503	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	C2	J1
O C R504	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	C1	J1
O C R505	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	C2	J2
O C R506	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	C2	J2
O C R507	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	C2	J2
O C R508	31218-0101	RESISTOR, Carbon Film, 110 ±5%, 1/4w	C2	J2
O C R509	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	B3	J3
O C R510	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	B3	J3
O C R511	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	B3	J3
O C R512	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	B3	J3
O C R513	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	B3	J4
O C R514	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	B3	J4
O C R515	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	B3	J4
O C R516	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	B3	J4
O C R517	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	H1	J5
O C R518	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	G3	J5
O C R519	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	G3	J5
O C R520	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	G3	J5
O C R521	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	H1	J6
O C R522	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	G3	J6
O C R523	31218-0221	RESISTOR, Carbon Film, 220 ±5%, 1/4w	G3	J6
O C R524	31218-0102	RESISTOR, Carbon Film, 1K ±5%, 1/4w	G2	F5
O C R525	31218-0102	RESISTOR, Carbon Film, 1K ±5%, 1/4w	G1	E5
O C U501	74248-0574	I.C. 74HC574 Octal 'D' Flip-Flop	D2	H1
O C U502	74253-0003	I.C. ULN-2803A Transistor Array	C2	I2
O C U503	74248-0574	I.C. 74HC574 Octal 'D' Flip-Flop	D3	H3
O C U504	74253-0003	I.C. ULN-2803A Transistor Array	C3	I4
O C U505	74248-0574	I.C. 74HC574 Octal 'D' Flip-Flop	E3	H5
O C U506	74253-0003	I.C. ULN-2803A Transistor Array	F3	I6
O C U507	74065-0002	I.C. 555 Timer	F1	E5